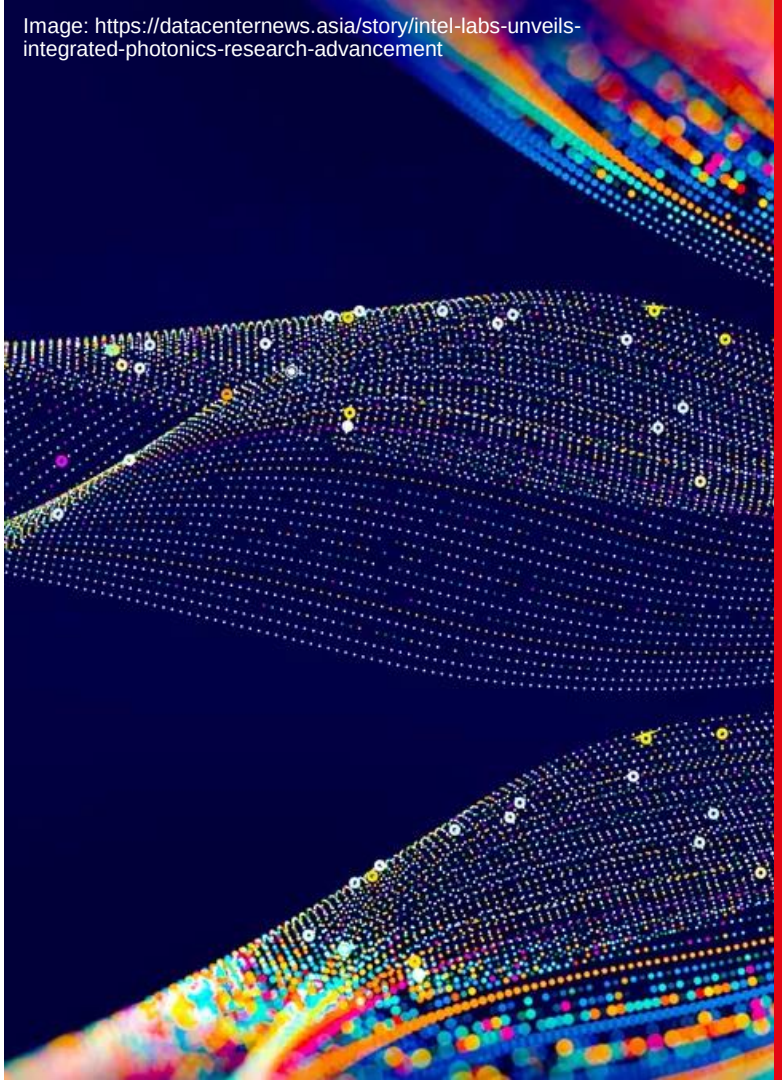


Image: https://datacenternews.asia/story/intel-labs-unveils-integrated-photonics-research-advancement

Beyond CMOS: Integrated Photonics

Kirsten E. Moselund, EPFL & PSI

Second of two lectures today

10:45 – 12:15 CMOS emerging architectures

- Technology scaling
- Transistor architectures
- CMOS processing

Computation

14:00 – 15:30 Beyond CMOS: Integrated Photonics

- Interconnect bottleneck
- Optical communication
- Photodetectors and Emitters on silicon

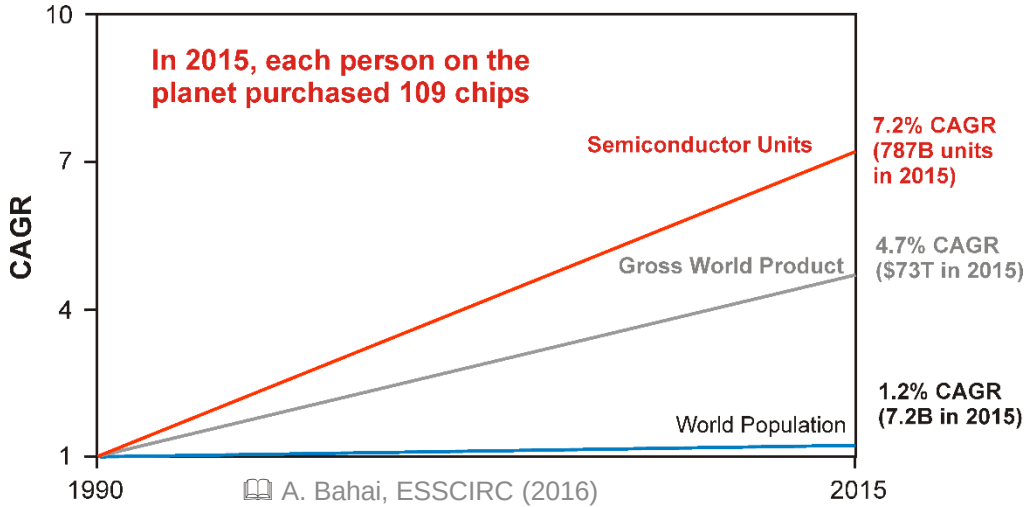
Data transmission

Questions welcome anytime – please interrupt me!

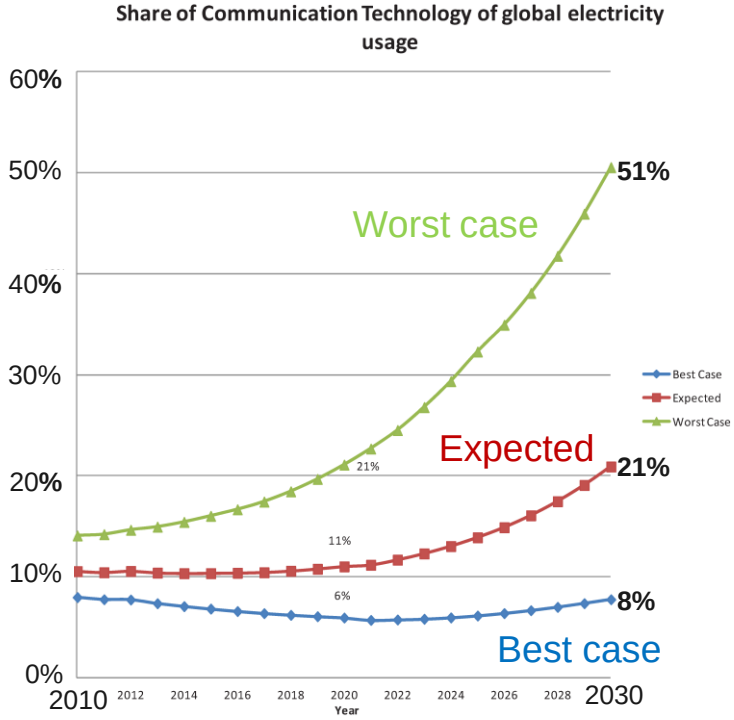
Integrated Photonics - Overview

- Interconnect bottleneck
- Optical communication
- III-V integration on Silicon
- Photodetectors
- Emitters

Number of chips are increaseing



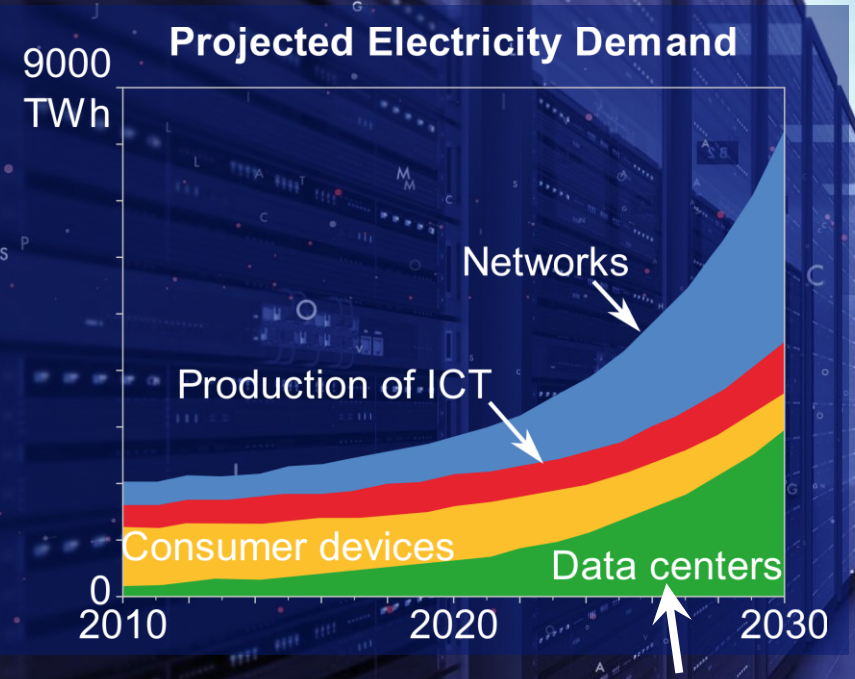
📖 A. Bahai, ESSCIRC (2016)



📖 Andrae & Edler,On Global Electricity Usage of Communication Technology, 2015.

- Fraction of ICT power consumption is increasing
- Need to address power consumption at all levels

Global Data Traffic – The Zettabyte Era



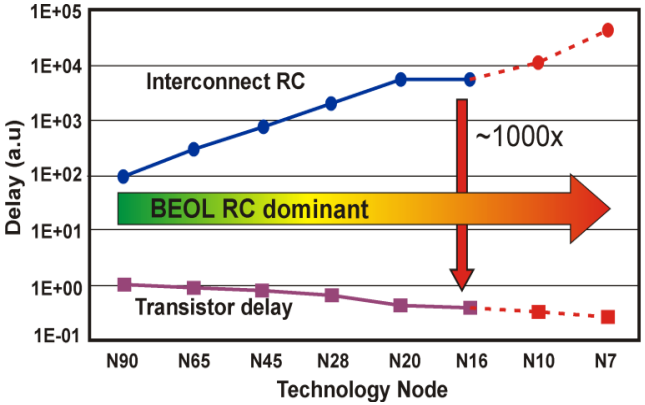
- **2% of world's electrical energy consumption**

14%	9%	77%
Data center – End user	Data center – Data center	Within data center

→ Need to reduce energy per bit

Jones, Nature, 2018
Cisco Global Cloud Index, 2015–2020
Patterson, Chip Scale Review, 2017

Interconnect bottleneck



📖 http://www.monolithic3d.com/blog/qualcomm-scaling-down-is-not-cost-economic-anymore-so-we-are-looking-at-true-monolithic-3d

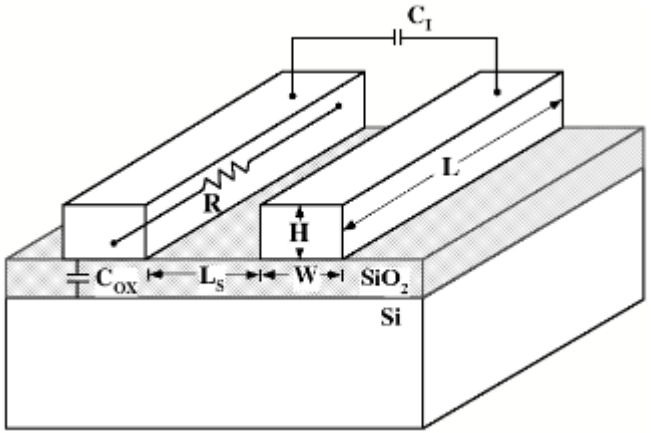
Interconnect increasingly dominates system level performance. Interconnect > 50% of power consumption.

➔Interest in photonic interconnect.

➔ Scaling of photonics towards elecronics

- Current advanced photonic devices are on the 100s of μms scale
- New device architecture for on-chip photonics needed

Interconnect scaling



$$R = \rho \frac{L}{WH}$$

$$C_{ILD} = K_{ox}\varepsilon_o \frac{WL}{X_{ox}}$$

$$C_{IMD} = K_{ox}\varepsilon_o \frac{HL}{L_S}$$

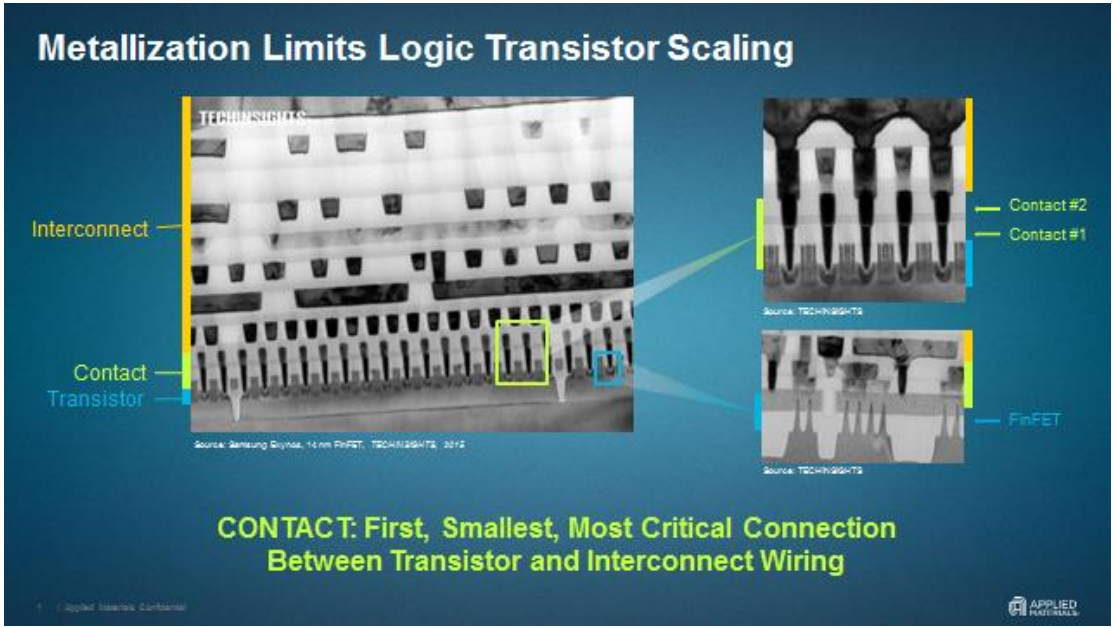
- Chip area increases with each node
- Device dimensions are scaled
- Scaled wires are:
  - Longer (chip area scaling)
  - Thinner (minimum dimension scaling

Interconnect parameters

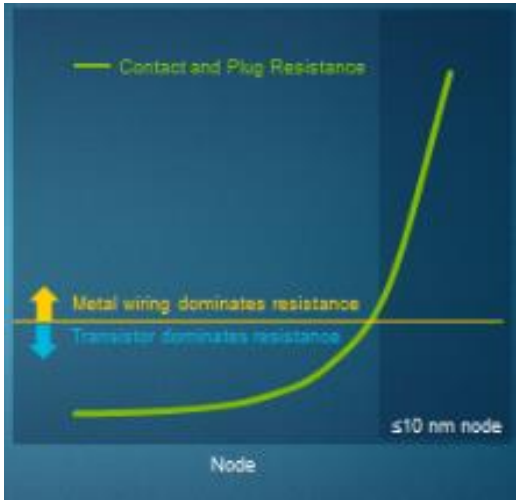
- L increases,
- X_{ox}, L_S, W and H decrease

→R, C_{ox} and C_I increase

Contact Resistance Limits Transistor Performance



- Shrinking interconnect cross-section
- Conductor volume decreases



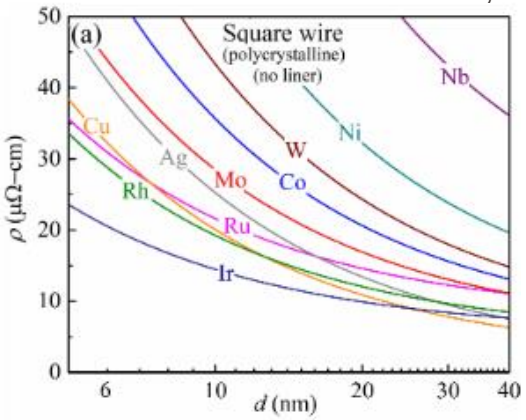
📖 https://blog.appliedmaterials.com/contact-resistance-and-its-role-limiting-transistor-performance

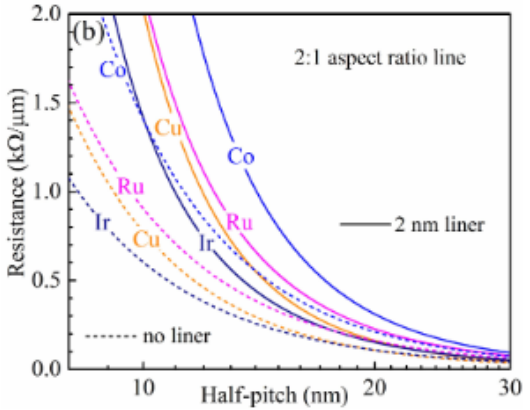
Technological solutions for metal interconnect

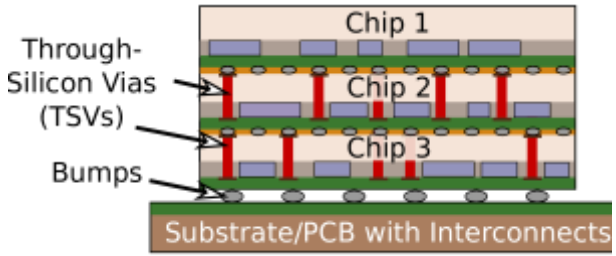
- Higher conductance metals → reduce R.
- Barrier-less interconnect
- 3D integration → reduce global length of interconnect
- Low-K inter-layer-dielectrics (ILD) → reduce C

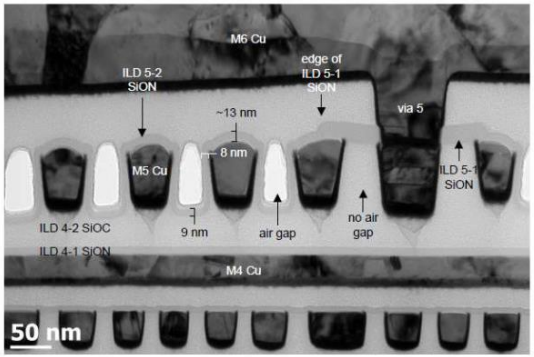
Each of these approaches make for a full lecture

📖 J. Gall, J. Appl. Phys. 127, 050901 (2020).







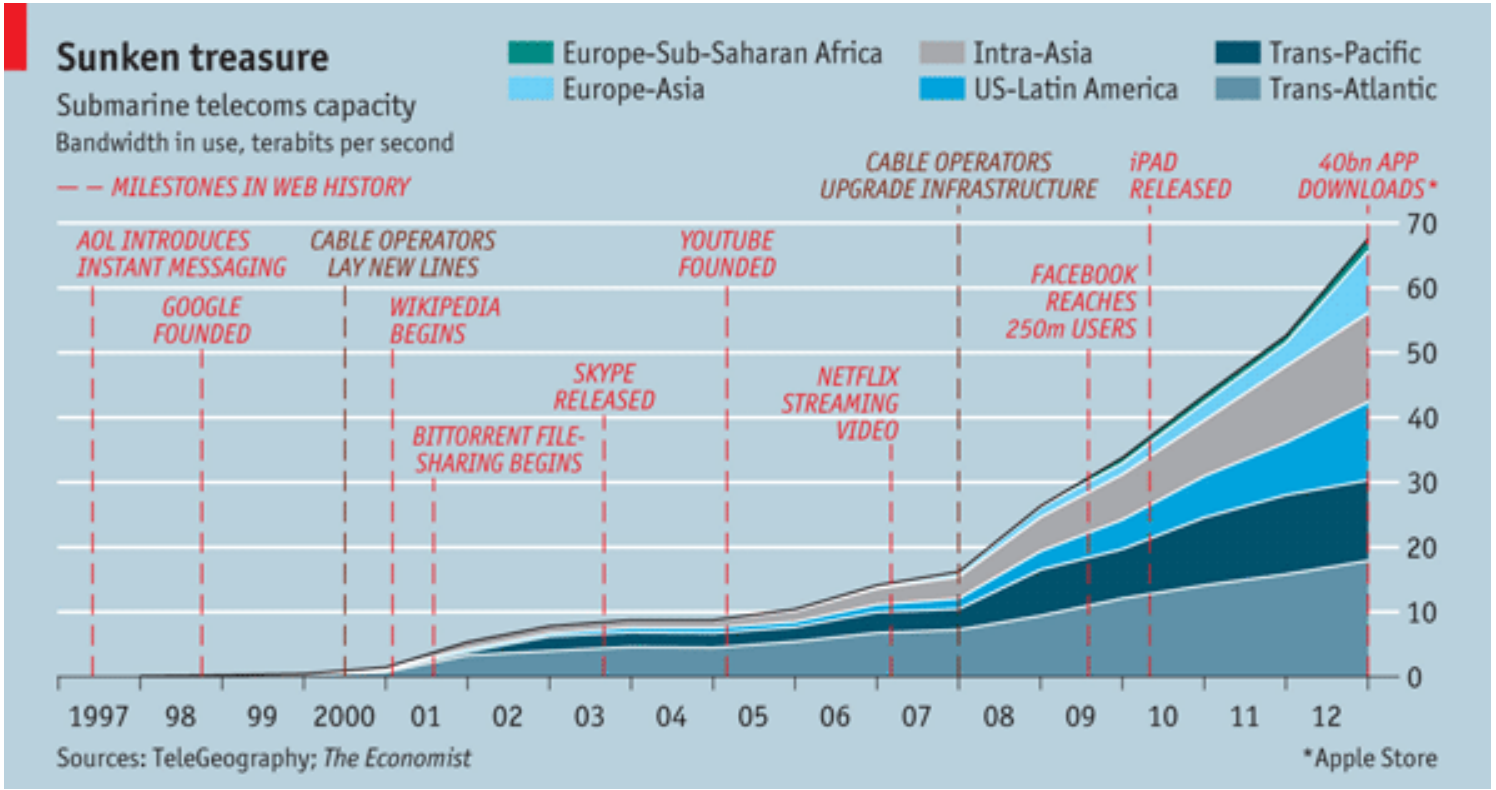


📖 P. Besser, NCCAVS Symp. 2017

chipworks

Optical Communication

The rise of the internet....

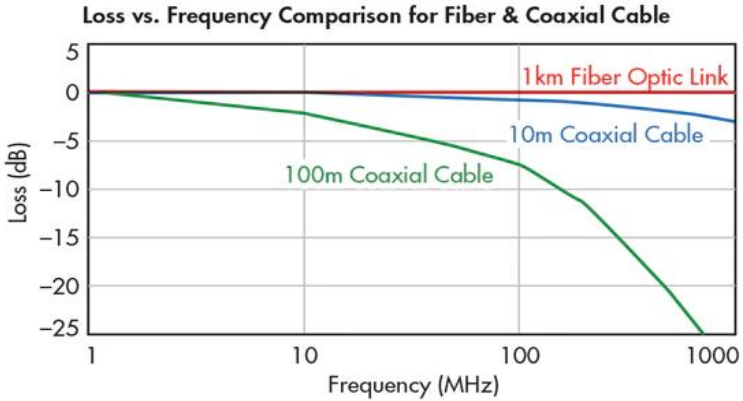


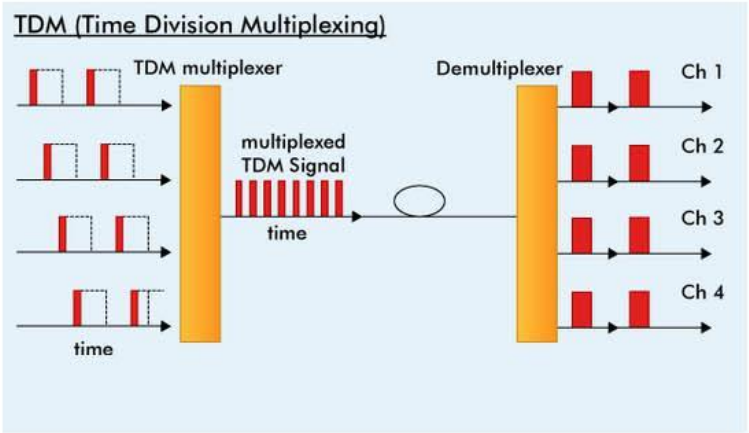
📖 Source: https://qeol.wordpress.com/2013/02/13/submarine-telecoms-capacity-and-the-rise-of-the-internet/

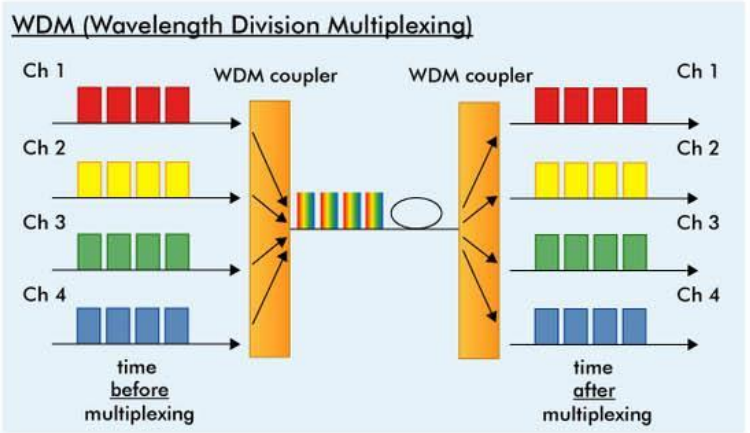
...Enabled by optical technologies

- Optical fiber technology
- Repeaters: Erbium-doped-fiber-amplifiers (EDFA)
- Wavelength-division-multiplexing.

📖 Courtesy of ViaLite



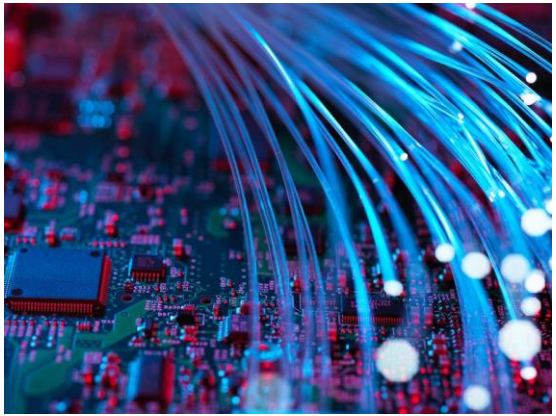




📖 https://www.pandacomdirekt.com/technologies/detail/tdm.html

Silicon Photonics Integrated Circuits

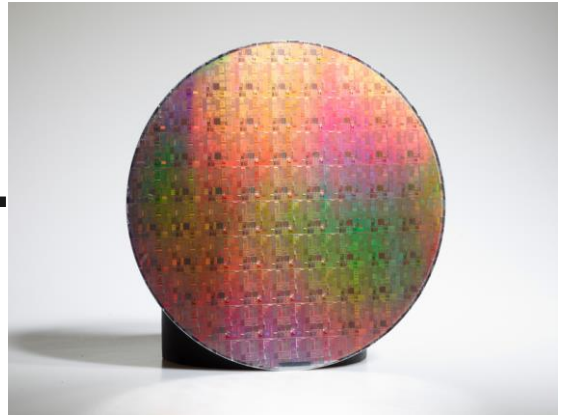
Optical communication



High speed,
large bandwidth,
low power

+

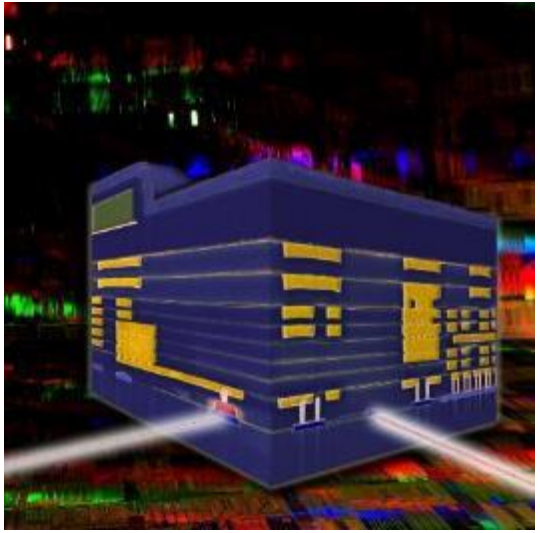
Silicon technology



Mature and cost-effective
Si technology

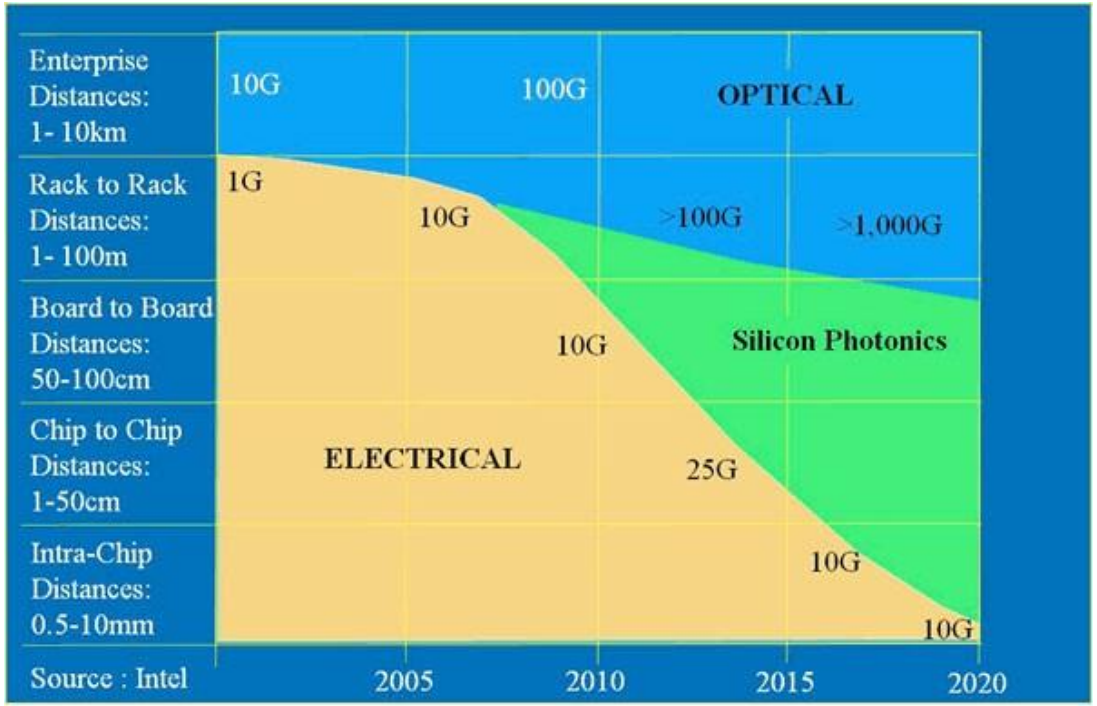
=

Silicon photonics
integrated circuits



Source: IBM Research

When will photonics replace electrical interconnect?



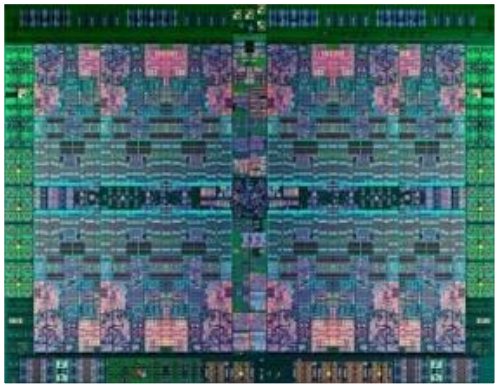
📖 Source: Photonics 21, WG6 Workshop, 2013

- Technological challenge – light source
- Cost challenges - integration
- Size-discrepancy electronics >< Photonics
- Power challenge – low power photonic components.

Integration density

Electronic Chip

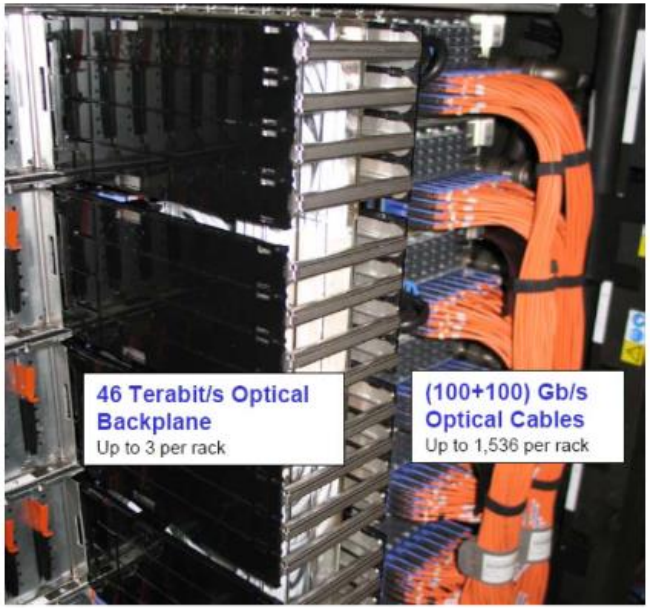
IBM P8 Processor



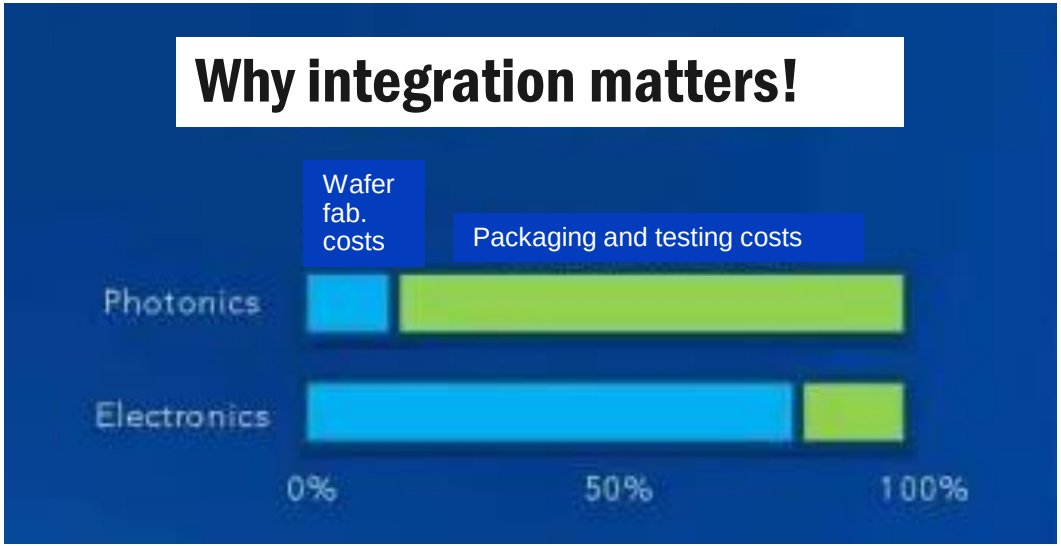
~ 650 mm²
22 nm technology , 16 cores
> 4.2 Billion Transistors

Optical Backplabe

High-performance computing



📖 A. Benner “Optical Interconnect Opportunities in Supercomputers and High End Computing”, OFC 2012



📖 **https://rainerklute.wordpress.com/2018/08/31/poet-technologies-agm-2018/**

- Packaging and testing are a large fraction of cost of conventional photonic devices
- Integration of devices is the only effective means of
  - Improve size, power, cost, speed, reliability and scalability
  - Enable new functionalities
  - Drive disruption in optical communications

Advanced Manufacturing
Technology Transfer Centers

Proposal I am working on right now

Swiss Photonics Integration Technology Center (Swiss PITC)

LIGENTEC · PAUL SCHERRER INSTITUT PSI · EPFL · SWISS PHOTONICS · POLARITON TECHNOLOGIES · OST

Application spaces addressed and targeted growing end-customer markets

- Atomic clocks
- Optical communication
- Photonic quantum computing
- Automotive
- Miniaturized laser systems
- Industrial measurement systems
- Miniature clinical diagnostics systems

Customer solution architecture space

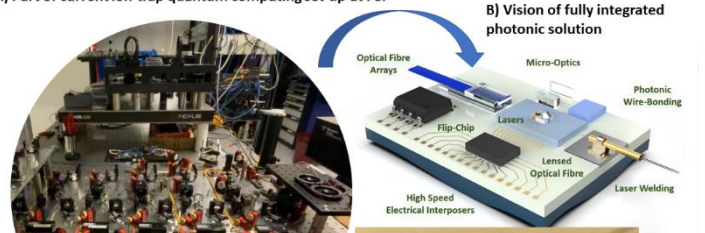
- Photonic integrated circuits
- Quantum photonics packaging
- MOHPS
  Micro-optical hybrid photonic systems

Service offering as controlled high MRL production workflows

- Design
- Wafer backend processing
- Precision pick & place
- Fiber to chip alignment
- Encapsulation

A) Part of current ion-trap quantum computing set-up at PSI

B) Vision of fully integrated photonic solution



C) Qubit control through a waveguide array coupled to a fiber bundle

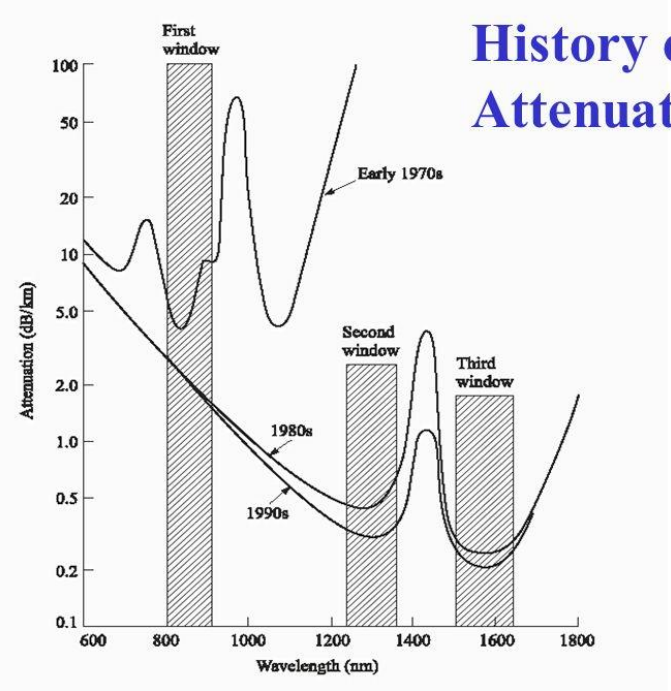
PIC schematic taken from: "Bundalo et al. IEEE J. Select Top. Quant. Electron, vol. 28, 2022"

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

ETH BOARD

Communication wavelengths

Optical fiber (OF) transparency



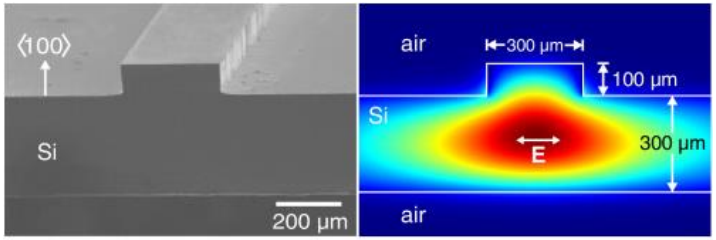
- First window – greatest optical fiber transparency at that time
- First GaAs-based LEDs/lasers
- Second window still used for datacom
  - O-band (original) 1260 to 1360 nm
  - Better for Ge detectors
- Third window = main telecom band
  - C-band (conventional) ("erbium window") - 1530 to 1565 nm

Transmission on-chip

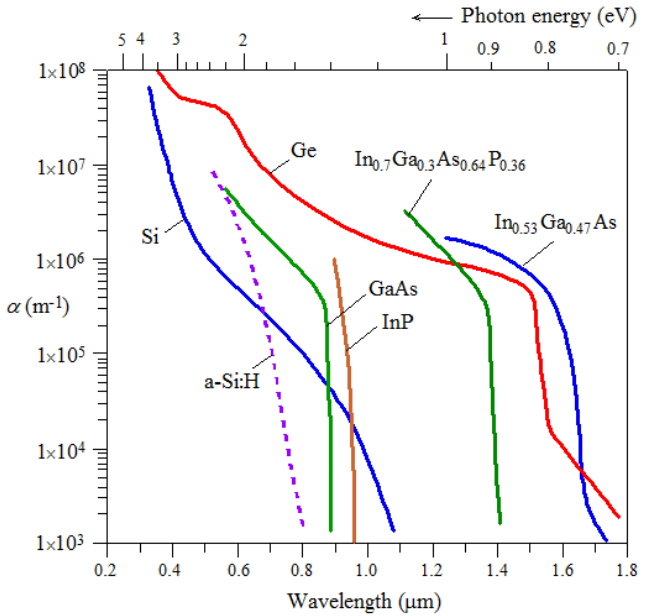
📖 S. Li et al. Optica, 2015.

Silicon waveguides on-chip

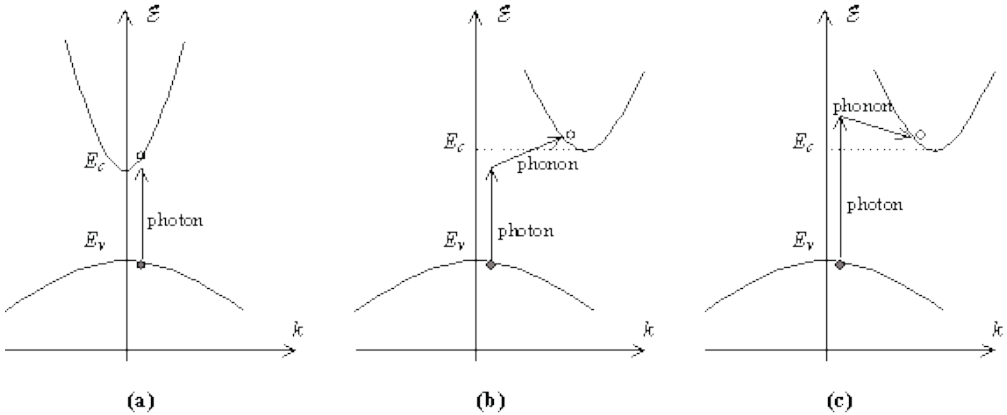
- Si is transparent above ~1.1 μm wavelength
- Very low-loss transmission
- Rib – or SOI nanowire Waveguide, multiplexers, splitters etc.
- No issues with cross-talk
- But, indirect bandgap – no light emission!

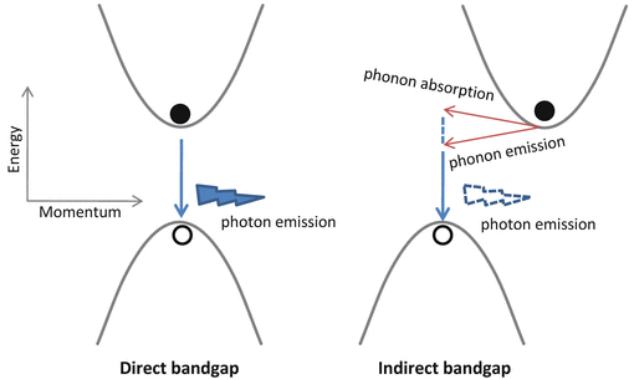


(a) (b)



Optical transitions





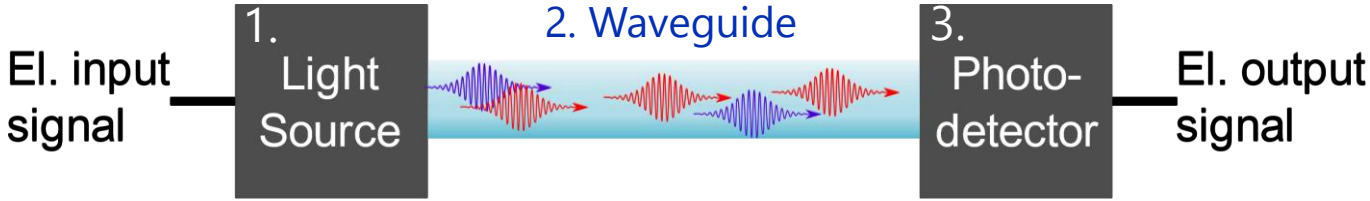
Absorption – photodetection

- Possible, but less efficient in an indirect bandgap material
- Silicon is an adequate detector in the visible (CCD camera's)

Photon emission

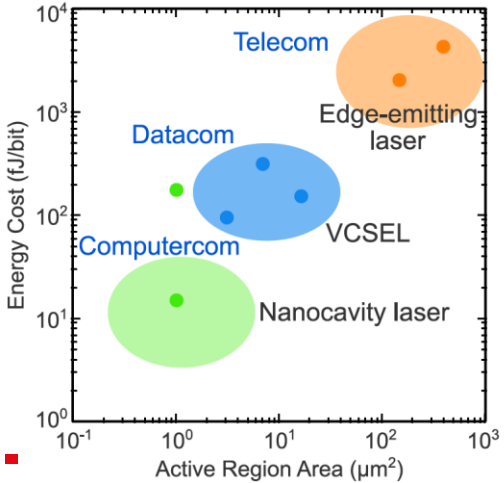
- Very unlikely in an indirect bandgap material
- Silicon cannot be used to make a laser

The Challenges of Silicon Photonics Integrated Circuits



Energy (optical link)< Energy (electrical line)

Energy (light source) + Energy (photodetector)< 200-20 fJ/bit



→ Integration of gain material

→ Scaled optical devices

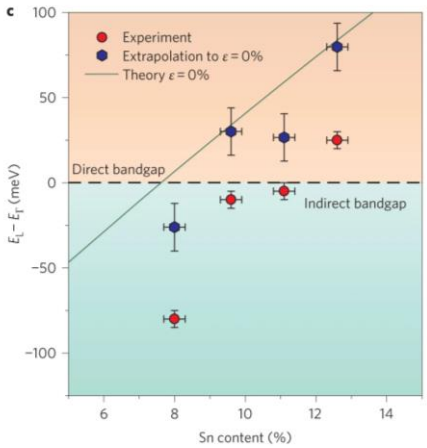
→ Short connections to electronics (close integration to Si electronics)

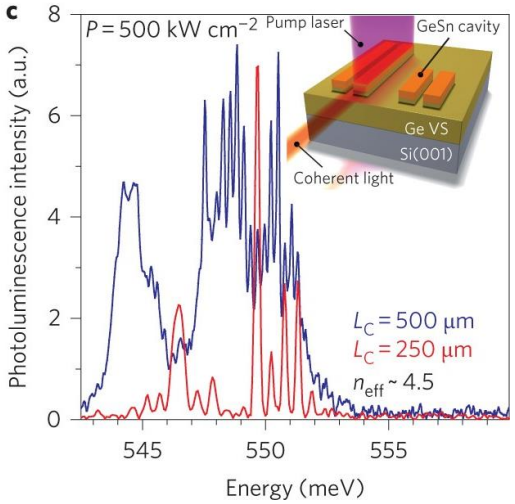
D. Miller, J. Light. Technol, 2017

T. Kakitsuka, S. Matsuo, NTT Tech. Rev. 10, 2–7, 2012

Group-IV based emitters: GeSn

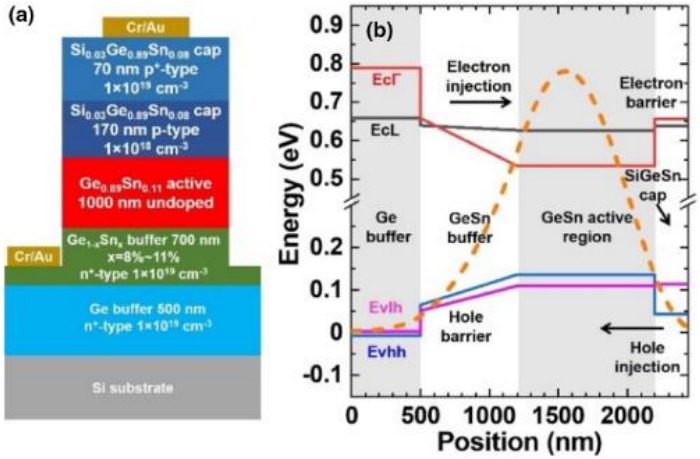
2015





- Optically pumped lasing
- Notoriously difficult to dope

2020

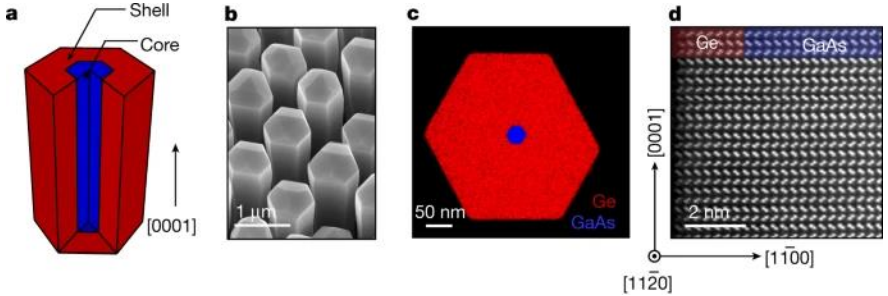


📖 Y. Zhou et al. Optica, 2020

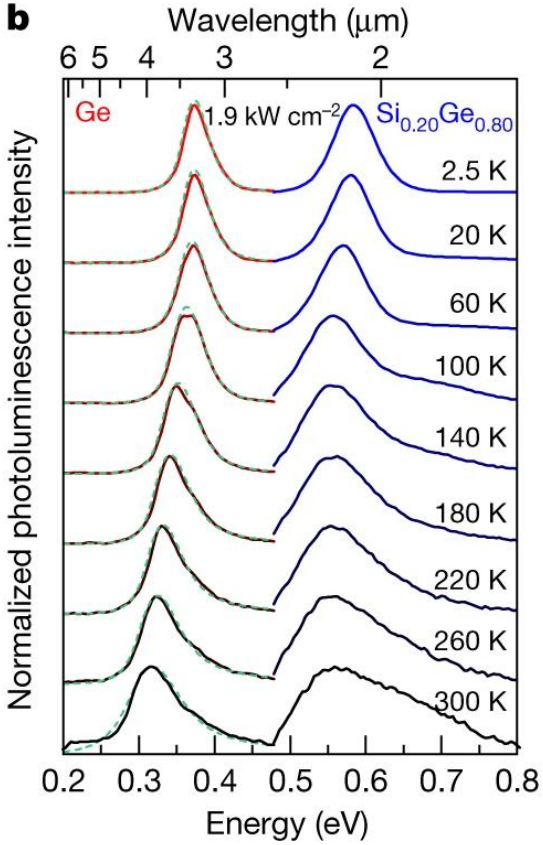
- Electrically pumped lasing, but only at <100 K

Group-IV based emitters: Hexagonal Si

- Zincblende is the preferred crystal phase for group IV
- Wurtzite crystal phase SiGe – posses region of direct bandgap
- Is energetically unfavorable to grow → exists in NW geometry only



📖 E. Fadaly et al. Nature, 2020



Photonic Integrated Circuit

Silicon transparency window → $\lambda > 1.1\ \mu m$
(O- and C-bands 1.38 & 1.55 μm)

Laser

- III-V material
  - Heterostructures needed for efficient laser
  - High-Q cavity
  - Applications for non-coherent emission (LED)
- Possibly off-chip
  - On-chip modulator

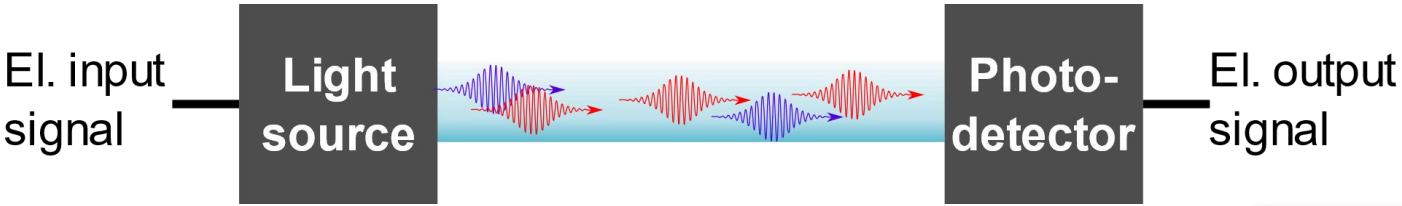
Transmission

- SOI waveguides
  - High index contrast 3.45 vs 1 (air)
- SiN
- Polymer waveguides

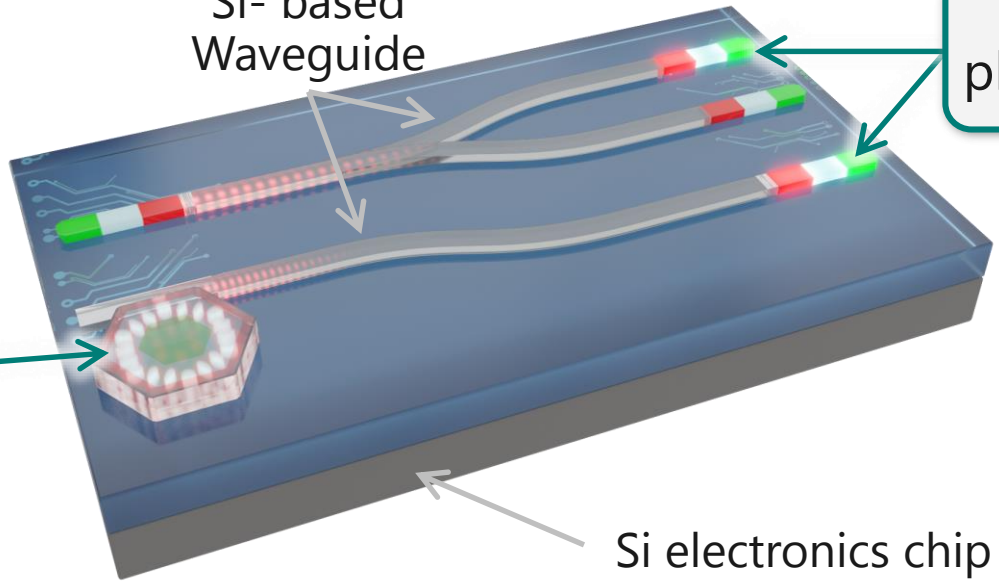
Detection

- Ge-based
  - Group IV
  - CMOS compatible
- III-V based
  - Direct band
  → more efficient
  → can be smaller

Towards a PIC in-plane integrated with Si



Si for transmission requires NIR wavelengths



Examples of available energy budget

Available energy

TABLE I
ENERGIES FOR COMMUNICATIONS AND COMPUTATIONS

Operation	Energy per bit	References and notes
Wireless data	10–30 μJ	[31]
Internet: access	40–80 nJ	[8]; (a), (b)
Internet: routing	20 nJ	[9]; (c)
Internet: optical WDM links	3 nJ	[32]; (d)
Reading DRAM	5 pJ	[5]; (e)
Communicating off chip	1–20 pJ	[5], [15], [16]
Data link multiplexing and timing circuits	~2 pJ	[24]
Communicating across chip	600 fJ	[5]; (f)
Floating point operation	100 fJ	[5]; (g)
Energy in DRAM cell	10 fJ	[33]; (h)
Switching CMOS gate	~50 aJ–3 fJ	[4], [6], [34], [35]; (i)
1 electron at 1 V, or 1 photon @1 eV	0.16 aJ (160 zJ)	

📖 D. Miller, J. Lightwave Tech. 2016

- To be competitive with near-future electrical global on-chip interconnects, the system energy should be ~ 500 fJ/bit.
- Individual devices can only be a fraction of this 1-10 fJ/bit
- Need to scale device volume and dimensions to reduce capacitance
- Complex trade-offs
  - Example: On-chip lasers burn energy, but allow for a more decentralized and flexible architecture

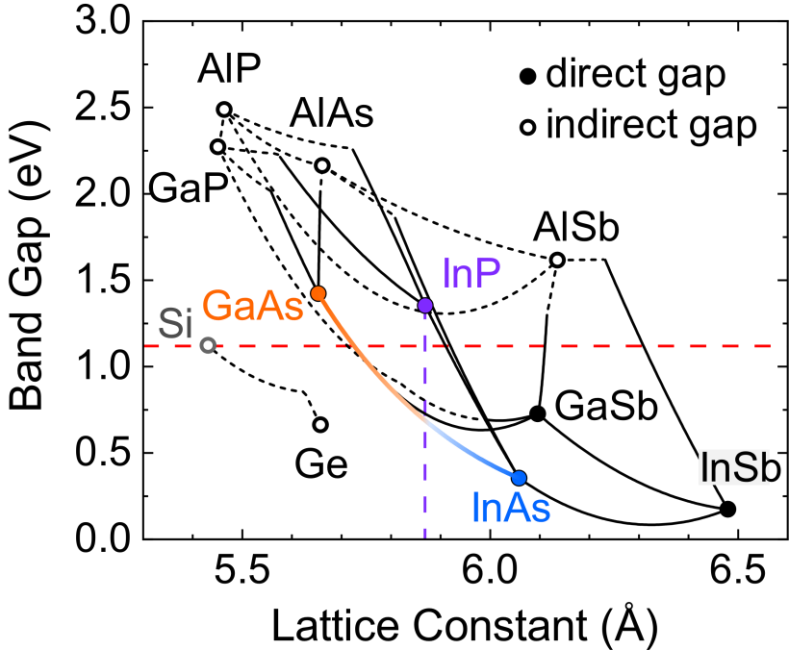
Partial Summary: Optical communication

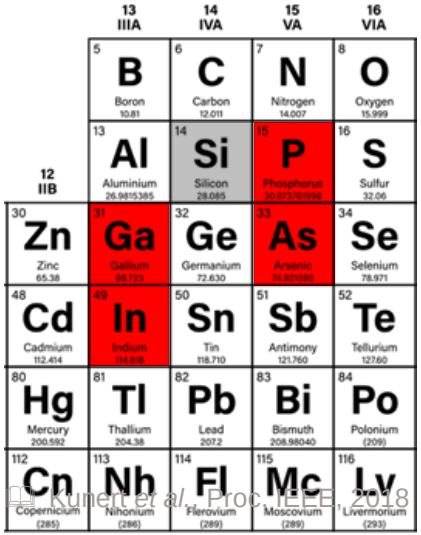
- Metallic interconnect is increasingly limiting chip performance
- Optical communication enabled the internet revolution
- Optical links are becoming increasingly favorable for shorter and shorter links
- On-chip optical communication is still not the norm, but is being explored in research
- Silicon is an ideal material for scaled optical wavegudies on-chip, but other materials are required for detection and emission above the silicon absorption band edge at 1.1 μm.
- On-chip optical communication requires very small power budgets of a few 100 fJ/bit to be competitive with electrical interconnect

III-V Materials Integration

III-V Materials

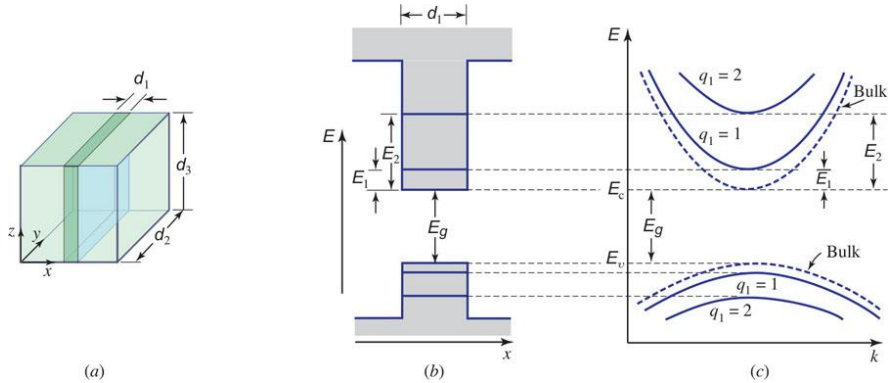
- Direct and tunable bandgap
- Enables both, emission and detection of light
- Currently used in telecommunication band





Kuneš et al., Proc. IEEE, 2018

Quantum wells – 1D infinitie potential well



Infinite 1D potential well Approximation

$$E_q = \frac{\hbar^2 (q\pi/d)^2}{2m}, \qquad q = 1, 2, 3 \ldots$$

- Double heterostructure, where the central layer has a smaller bandgap and is sufficiently thin that the energy levels are discretized
- The smaller the width of the well the smaller the separation between energy levels
- The well traps carriers → increases emission efficiency

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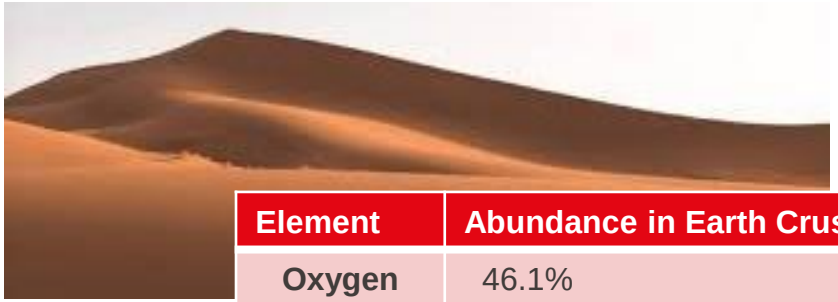
Motivation – Strengths and Limitations of Silicon

Silicon

- Cheap, abundant, self-passivating
- Material of choice for electronics
- Convenient band-gap
- >60 years of semiconductor technology

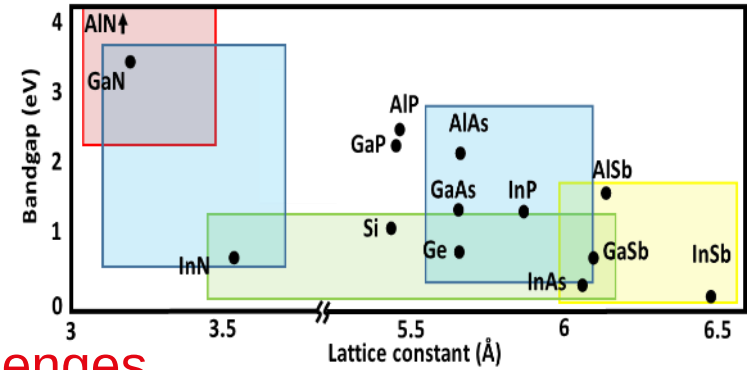
→ Silicon as technology platform



Element	Abundance in Earth Crust
Oxygen	46.1%
Silicon	28.2%
Indium	0.000016%

Opportunities for III-Vs

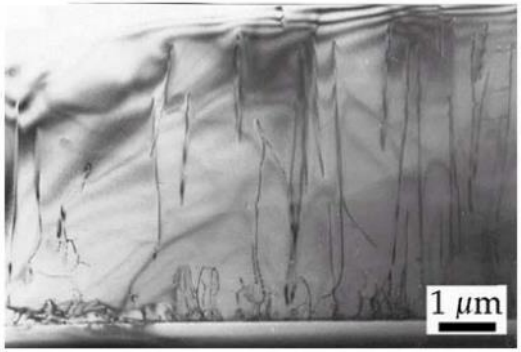
- Improved carrier mobility → InGaAs nFETs
- Heterostructures → steep-slope devices for low V_{dd}
- Direct band gap → III-V laser sources
- Tunable bandgap → low-power electronics, broad spectral range



→ III-Vs as technology booster

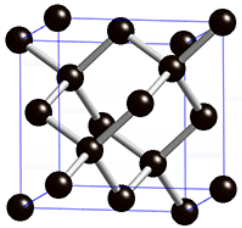
→ Material integration and process challenges

Challenges for III-V Integration on Si



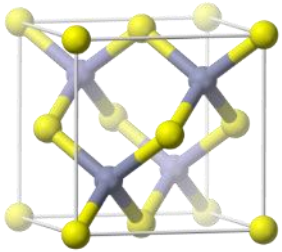
Threading dislocations in GaN layer
From: Awschalom group webpage UCSB

Si



Diamond structure

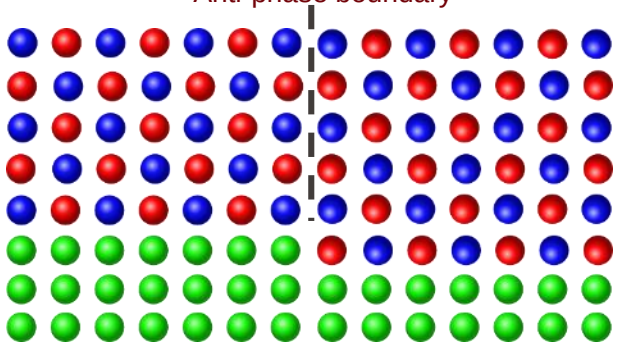
III-V



Zinc-blende structure

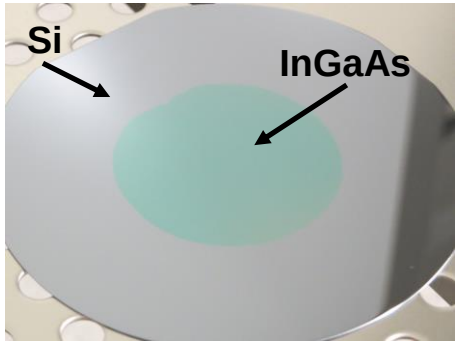
- **Lattice-mismatch** to Si: 3-13%
  → Threading dislocations
- Large **thermal expansion mismatch**
  - Growth at 500-700ºC
  - → Defects form when cooling
- **Crystal structure** difference
  → Anti-phase boundary defects

Anti-phase boundary

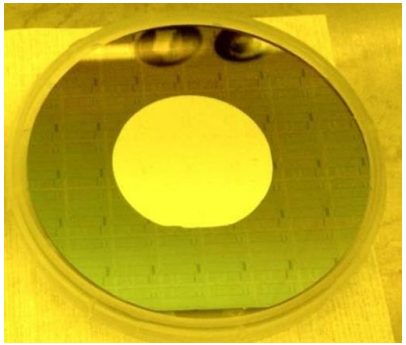


Wafer Bonding

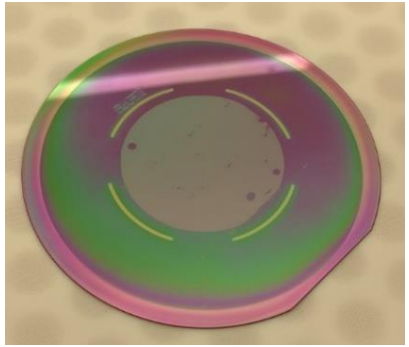
6 nm InGaAs on Si CMOS

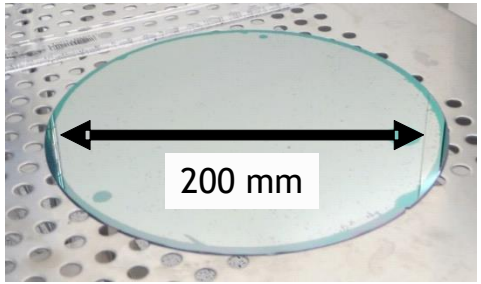


InGaAs on Si CMOS



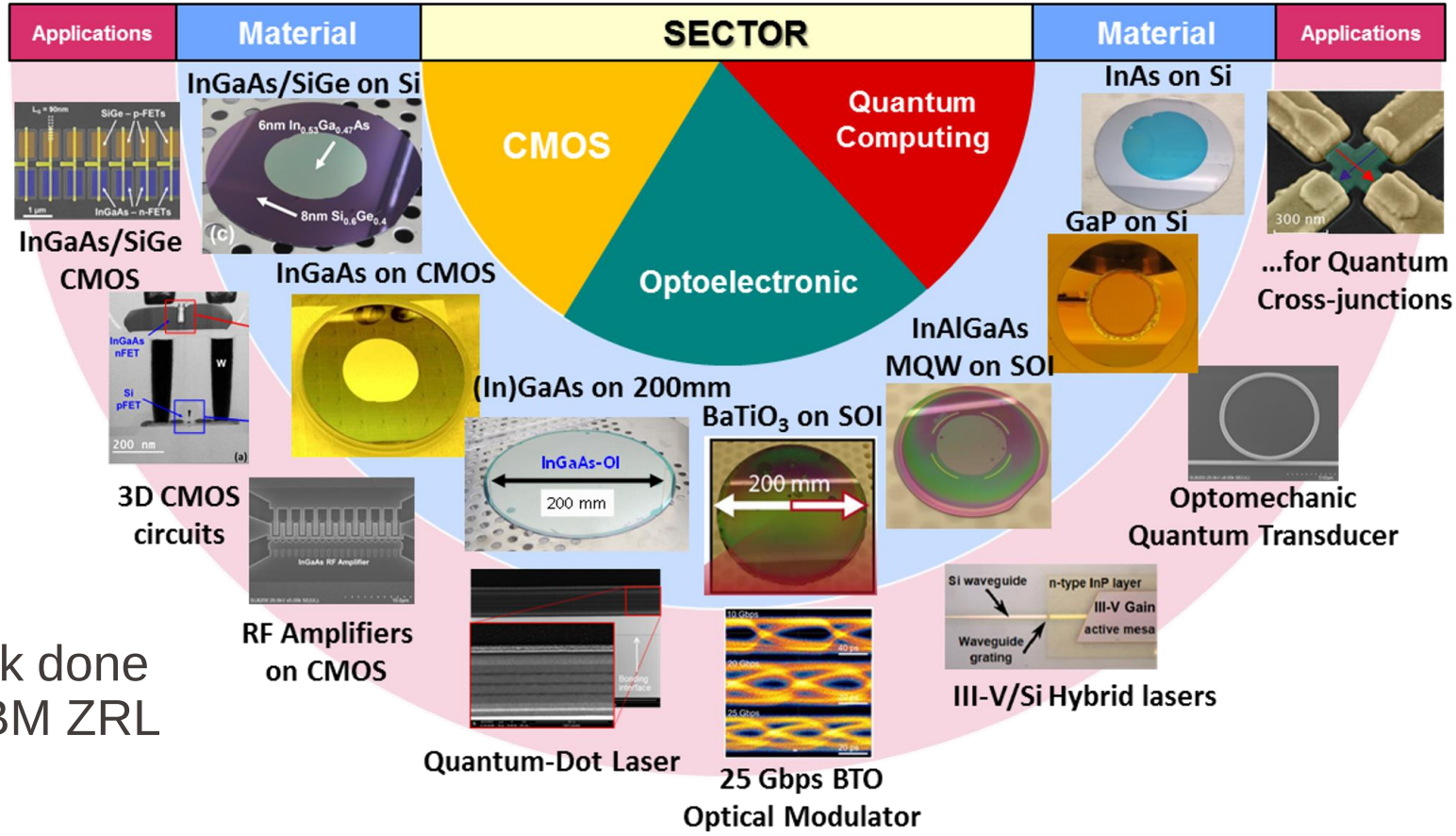
InGaAs on Si Photonics





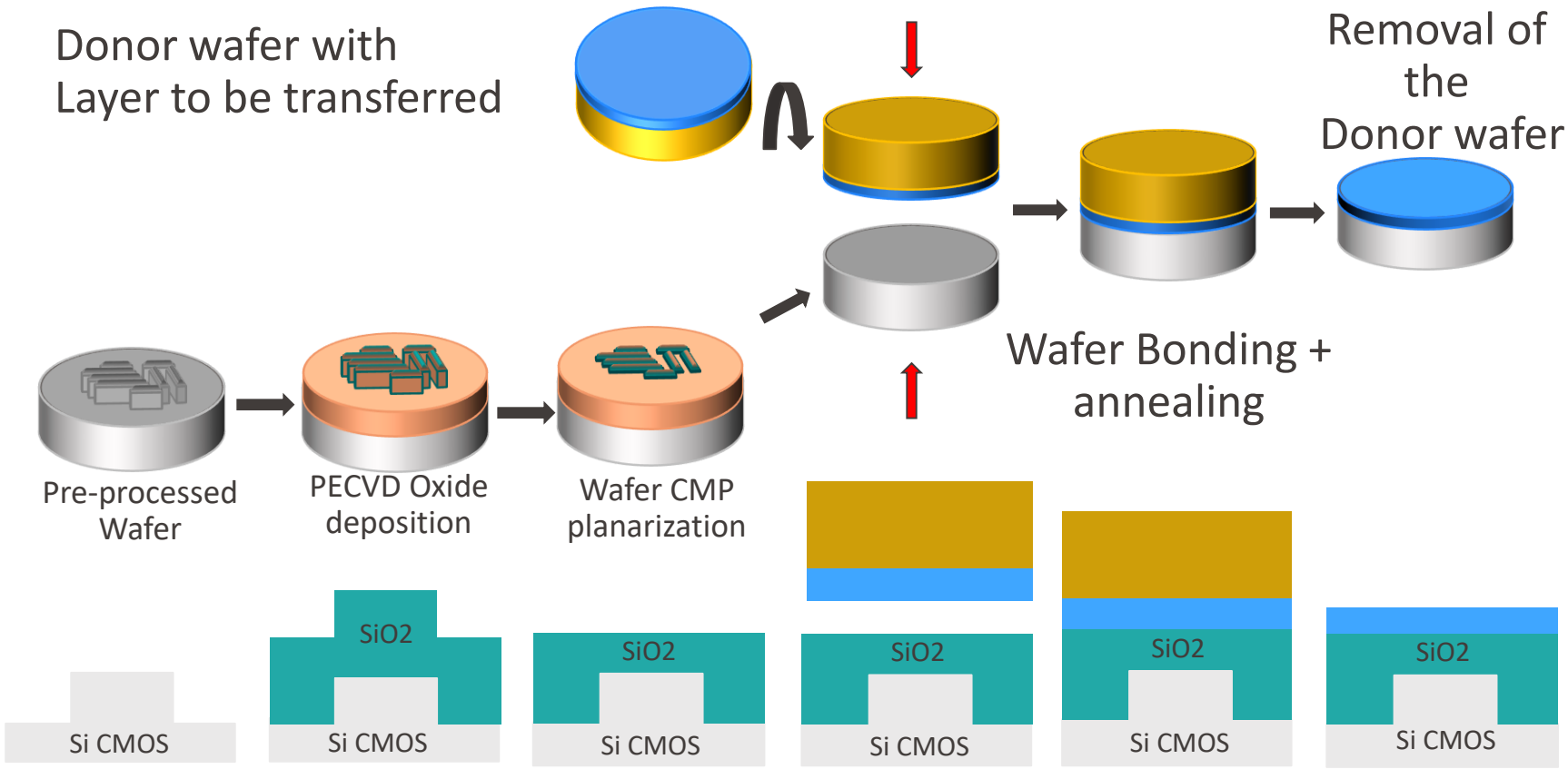
- Available to a wide range of materials
- Large scale wafer fabrication (200mm wafers demonstrated) – limited to the size of the III-V substrate?
- Suitable for Ultra-thin Body (UTBFETs) devices processing
- Immune to lattice mismatch
- Re-usable substrate

Direct Wafer Bonding (DWB) Applications Overview

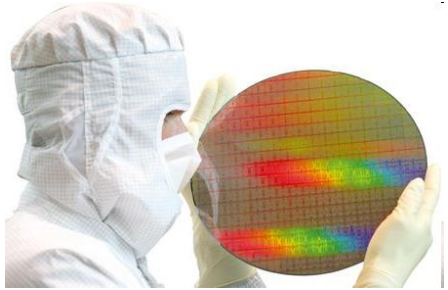


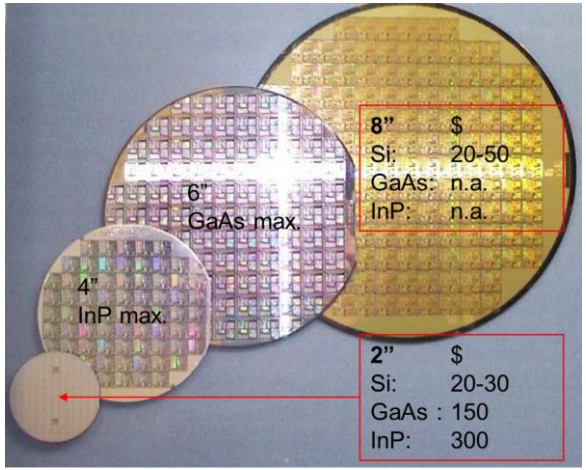
Work done at IBM ZRL

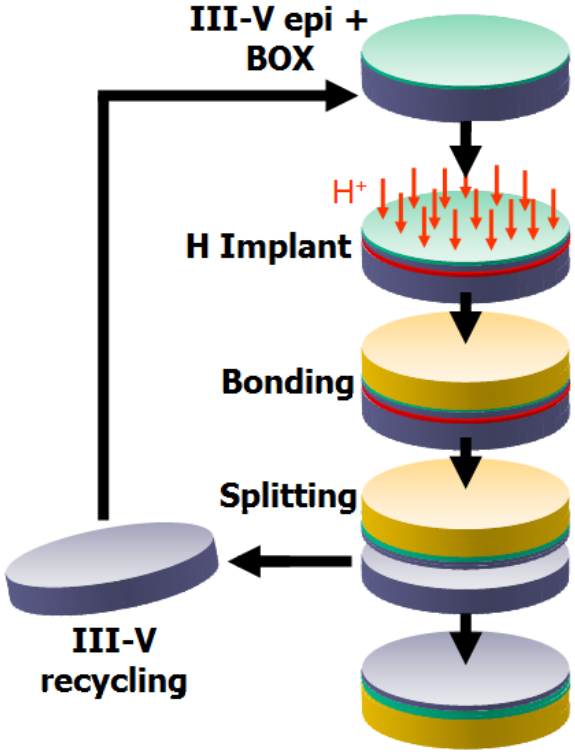
Direct Wafer Bonding on Pre-Processed Wafers



III-V Wafers Recycling







- H-induced donor wafer splitting
- Donor wafer recycling possible
- Cost-effective process

L. Czornomaz, et al., IEDM (2012)

Bonding of III-Vs on Si for Photonics

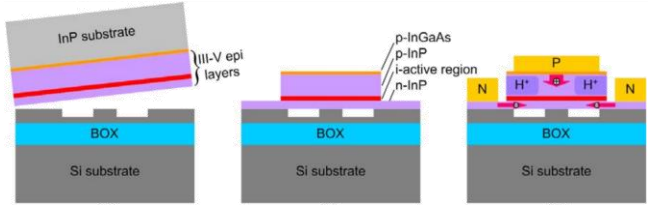
Benefits:

- Mature fabrication method
- High quality material
- High-performance devices demonstrated

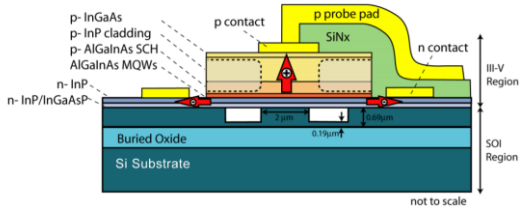
Challenges:

- Limited scalability to large wafer scale
- Multilevel coupling
- Processing of III-V more challenging than Si

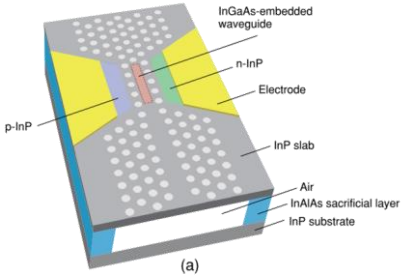
→ Long-term: Monolithic integration



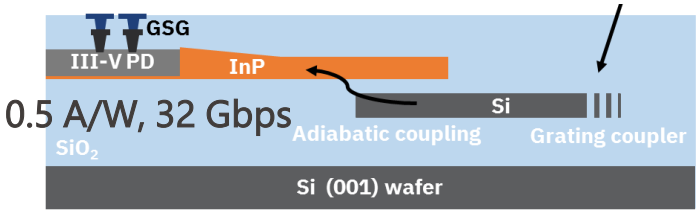
D. Liang et al., Materials 3, 2010



H. Park, et al. Opt. Exp, 2007



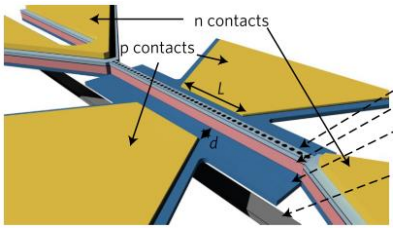
K. Nozaki et al., Optica, 2015



Baumgartner, OFC 2019

III-V epitaxy on Si for photonics

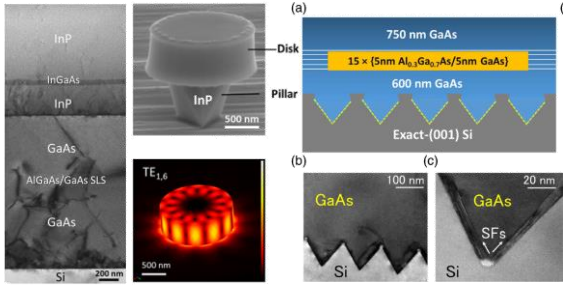
Wafer bonding



G. Crosnier, Nat. Phot. (2017)

- High material quality
- Dense integration challenges

Planar epitaxy



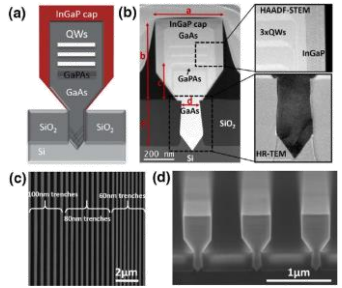
B. Shi, APL (2017)

Y. Wan, Optica (2017)

- Monolithic on Si
- Issues with material defects
- Topography

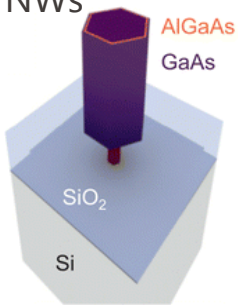
Selective epitaxy

Aspect-Ratio Trapping



Y. Shi, Optica (2011)

NWs



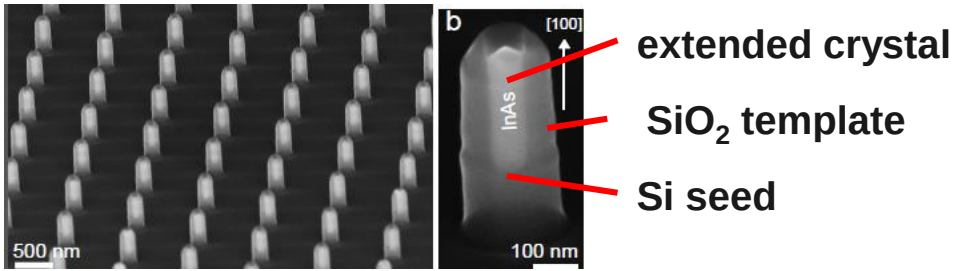
B. Mayer, Nano Lett. (2015)

- Scalable
- No thick buffers
- Geometry may be limiting

Template-Assisted Selective Epitaxy (TASE)

Concept

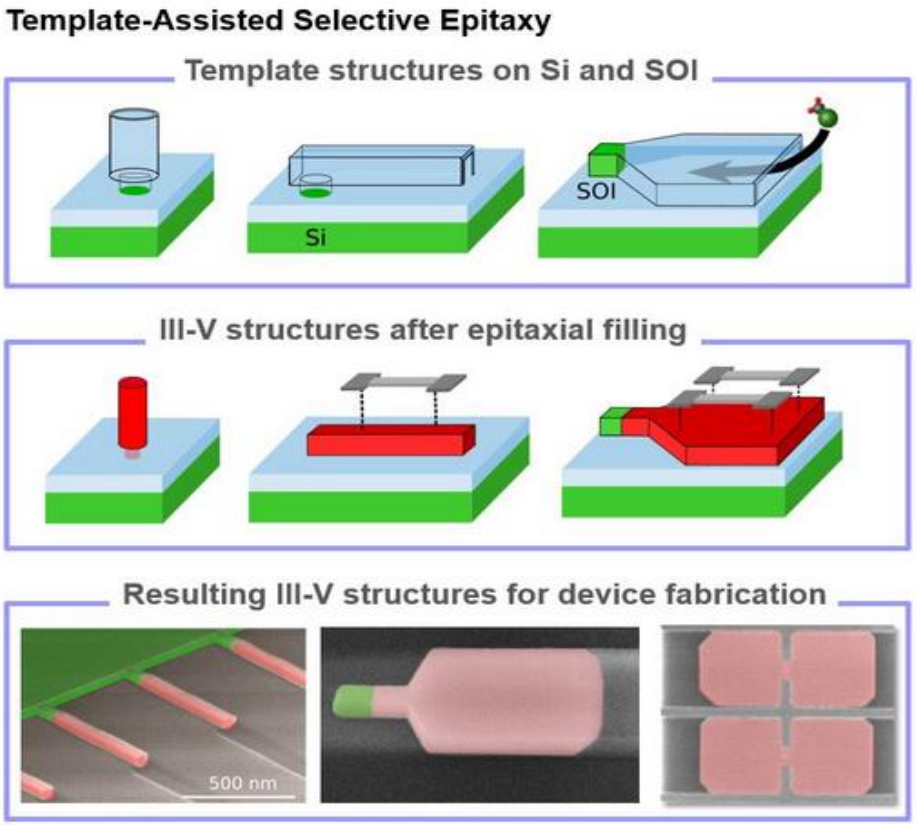
1. Start epitaxy from a single nucleation point
2. Keep area of epitaxial interface small
3. Expand seed and guide growth within oxide template



Nanoscale equivalent of Czochralski process (1916)

📖 Das Kanungo et al. (2013)
📖 Borg et al. (2014)
📖 H. Schmid et al. APL (2015)
📖 L. Czornomaz et al. VLSI (2015)

Template-Assisted Selective Epitaxy (TASE)



Benefits:

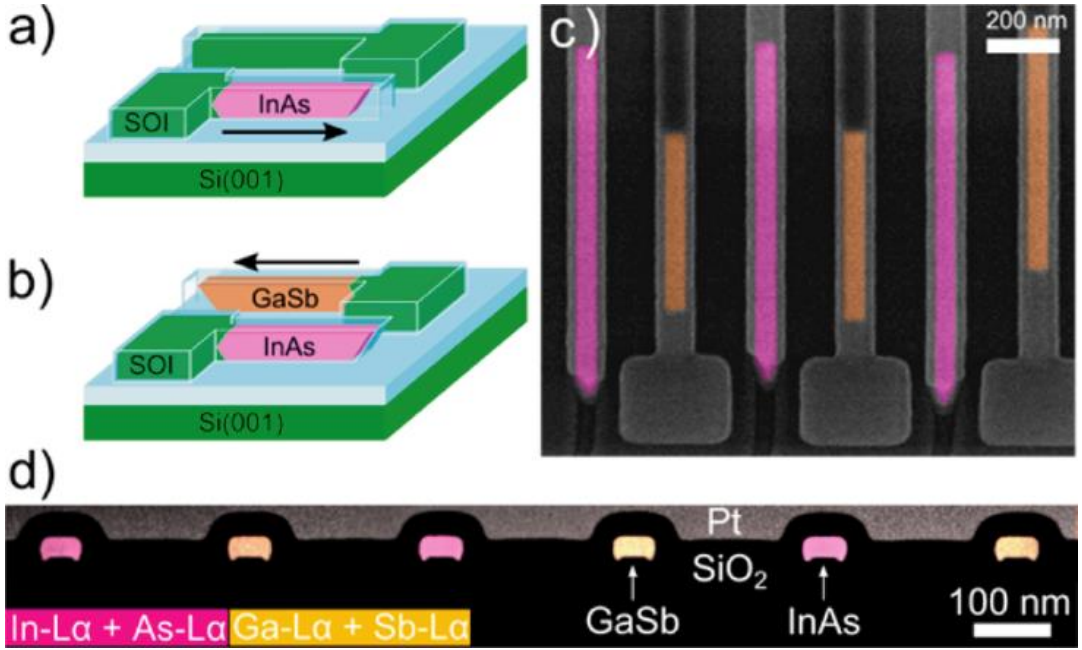
- Avoids lateral overgrowth of junctions associated with NW growth
- Self-aligned to other Si features
- In-plane homo- and hetero-junctions → avoids implantation or regrowth

📖 P. D. Kanungo et al. Nanotechnology (2013)
📖 M. Borg et al. Nano Letters (2014)
📖 H. Schmid et al. APL (2015)
📖 L. Czornomaz et al. VLSI (2015)

Co-Integration of multiple III-Vs

- Can repeat process to obtain different III-Vs and heterojunctions side-by-side.
- Requires multiple III-V runs for complementary devices.
- GaSb is option for p-channel III-V based complementary logic

Borg et al. ACS Nano 2017

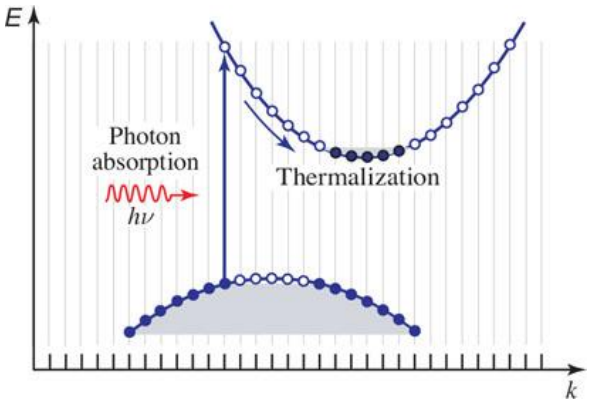


Partial Summary: III-V integration

- III-V material is required for the integration of optical emitters (Lasers and LEDs)
- III-V has a lattice mismatch of 3-12% wrt. Silicon, and thermal mismatch is also an issue in processing → defective material if grown directly
- Direct wafer bonding is the state-of-the-art method to get III-V on silicon
  - High quality material, same material all over the chip, evanescent coupling schemes
- Monolithic integration by direct epitaxy allows for local integration of III-V, but geometry is often limiting – nanowires etc.
- Template-Assisted Selective Epitaxy (TASE), presents a new opportunity to overcome some of these limitations

Detectors

Photon absorption



Momentum k-conserving absorption in indirect bandgap semiconductor

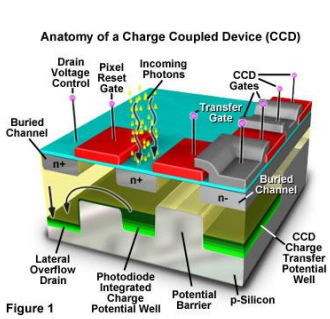
1) A photon generates an excited electron in the conduction band, leaving behind a hole in the valence band

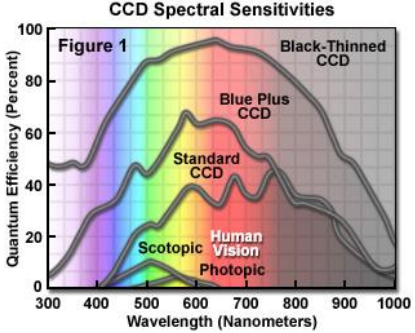
2) The carriers undergo fast transitions — to the lowest and highest available levels in the conduction and valence bands, respectively, releasing their energy in the form of phonons.

Sequential process → not unlikely.

Examples

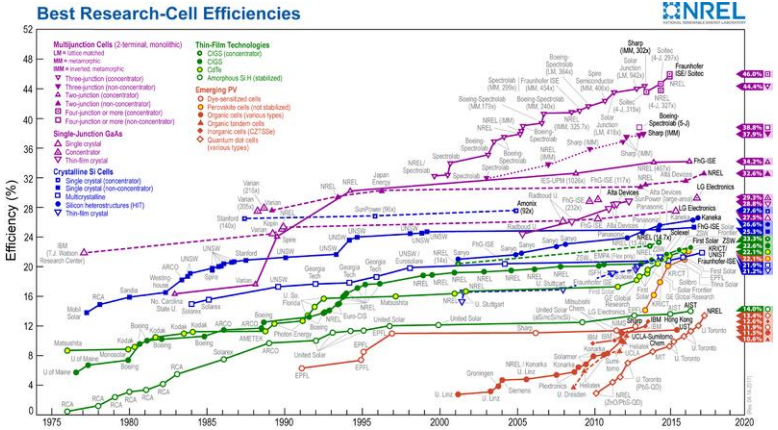
- Silicon image sensor





🕮https://hamamatsu.magnet.fsu.edu/articles/quantumefficiency.html

- Silicon photovoltaics



🕮https://commons.wikimedia.org/wiki/File:Best_Research-Cell_Efficiencies.png

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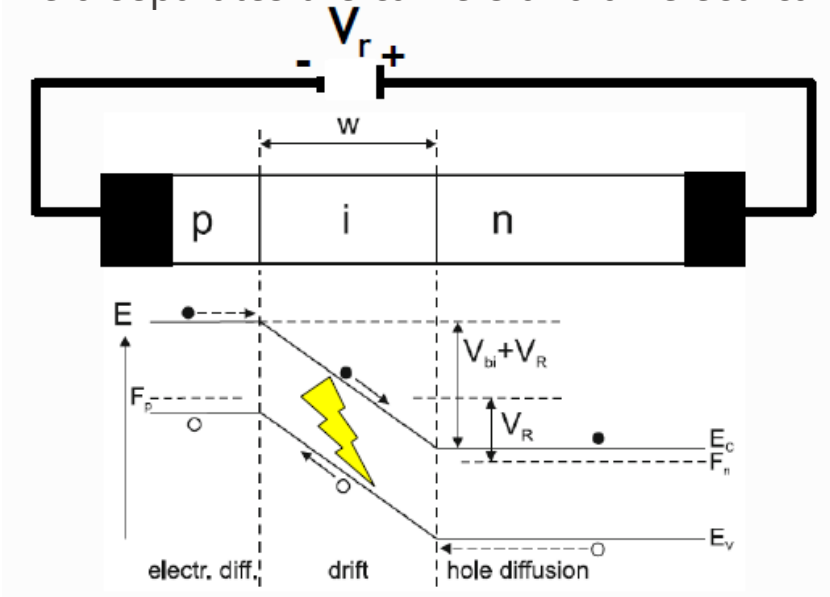
Photodiodes

- Converts an optical photon flux to electrical current
- Simplest case: reversed-biased *p-i-n* semiconductor junction
  - Photons absorbed in i-region
  - Reverse bias E-field separates the carriers and an electrical current flows



📖 M. Grundmann. Springer, (2015).

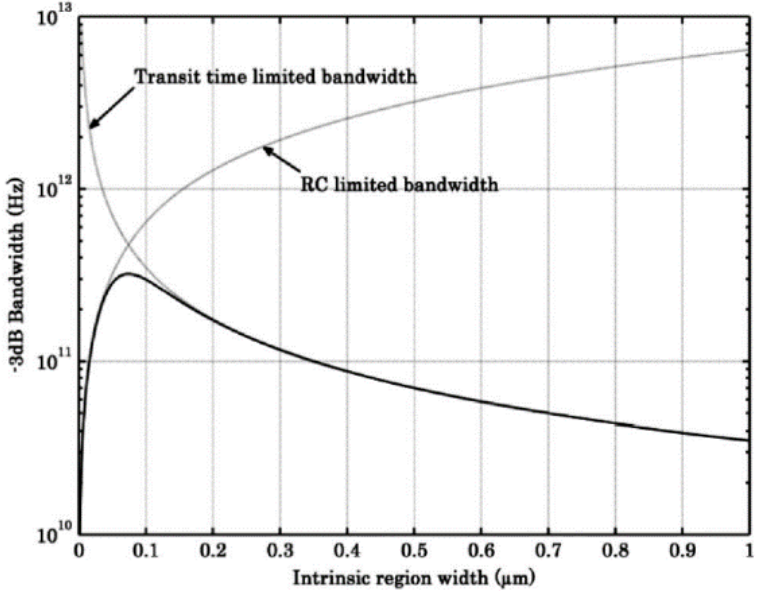
Photodiodes – Figures of Merit

- Dark current – reverse biased leakage (as low as possible)
- Responsivity [A/W] $R = \frac{\eta q}{hf} \sim \frac{\lambda_{(\mu m)}}{1.23985_{(\mu m \cdot W/A)}}$
- Bandwidth (speed)
  - Transit-time limited (the time to cross i-region

$$f_{3dB,tt} = \frac{0.45}{\tau_{tt}} = \frac{0.45 \cdot v_s}{W}$$

  - RC-limited

$$f_{3dB,RC} = \frac{1}{2\pi RC} = \frac{1}{2\pi(C_J+C_P)(R_S+R_L)}$$



📖 L. Virot, et al. Photon. Res. 1(3), 140, (2013).

Scaling the Optical Link – Photodetector

Requirements for PDs for PICs:

- → Low capacitance (<10fF)
- → Efficient detection → allows for smaller volumes
- → High responsivity
- → Close integration to Si electronics
- → Size matching electronics and photonics

TABLE IV
CAPACITANCE (C) OF SMALL STRUCTURES

Structure	C	References and notes
$100 \times 100\ \mu$m square conventional photodetector	~1 pF	(a)
$5 \times 5\ \mu$m CMOS photodetector	4 fF	[46]; (b)
Wire capacitance, per μm	~200 aF	[6]
FinFET input capacitance	~20–200 aF	[35]; (c)
$1 \times 1 \times 1\ \mu\text{m}^3$ cube of semiconductor	~100 aF	(d)
$100 \times 100 \times 100\ \text{nm}^3$ cube of semiconductor	~10 aF	(d)
$10 \times 10 \times 10\ \text{nm}^3$ cube of semiconductor	~1 aF	(d)

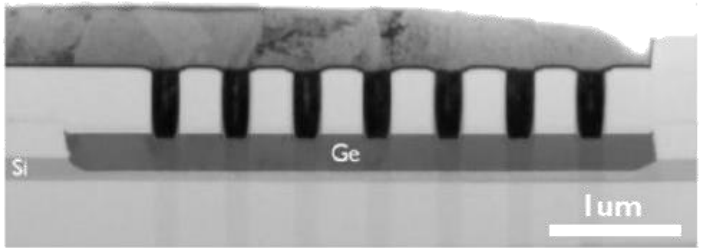
📖 D. Miller: J. Lightwave Tech. 2016

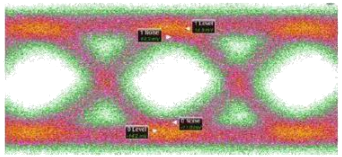
Germanium Photodetector

Ge-on Si photodetectors:

- State-of-the-art approach, CMOS compatible
- High-speed CMOS integrated photodetectors
- Waveguide coupled
- Indirect bandgap → reduces efficiency
- If you need the III-Vs for the emitter you might as well use it for detection

Germanium on Si Photodetector

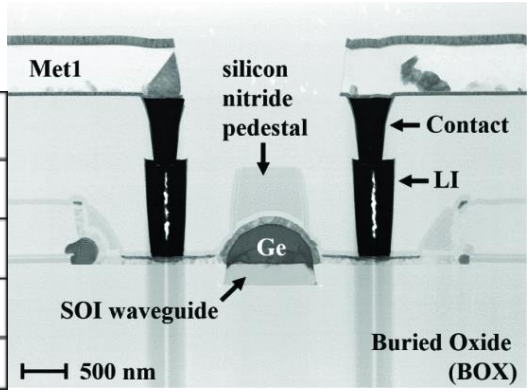


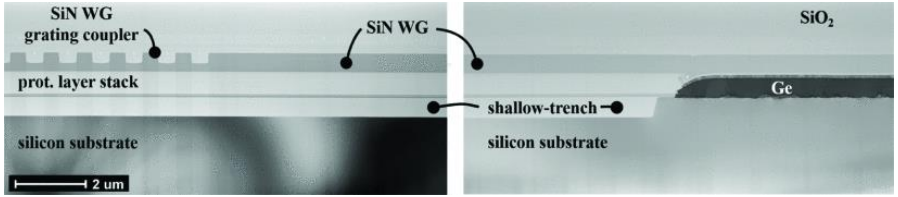


📖imec-int.com

📖S. Lischke, et al.
IHP, IEDM 2019

Parameter \ Platform	Bulk-Si with SiN WG [this work]
-3 dB bandwidth	> 67 GHz (-2 V)
internal resp. in O-band	0 3 A/W (-2 V)
internal resp. in C-band	*n/a*
dark-current	< 400 nA (-2 V)

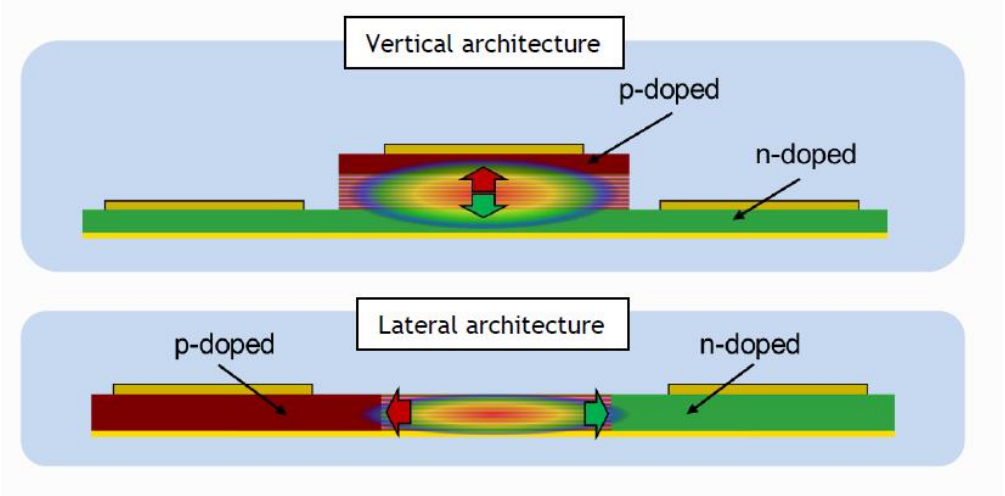


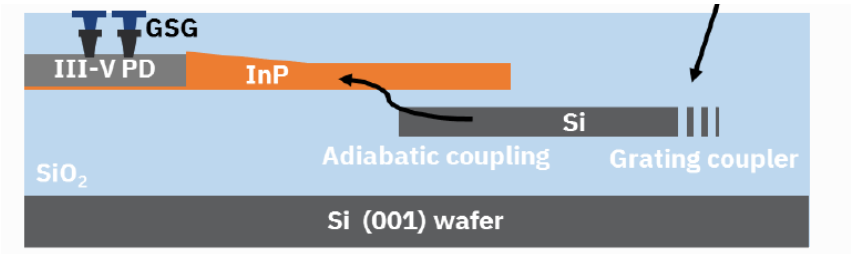


III-V based photodetectors

- Direct gap
  → high absorption
  → short devices
  → lower capacitance,
- low dark current and high mobility
- Increased efficiency in other telecom bands.
- Possible co-processing of light sources and detectors,

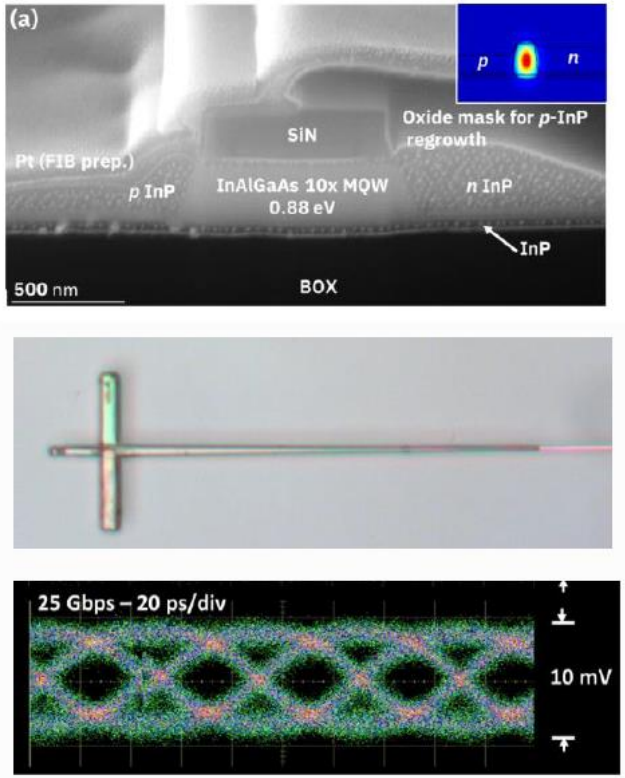
Different current schemes





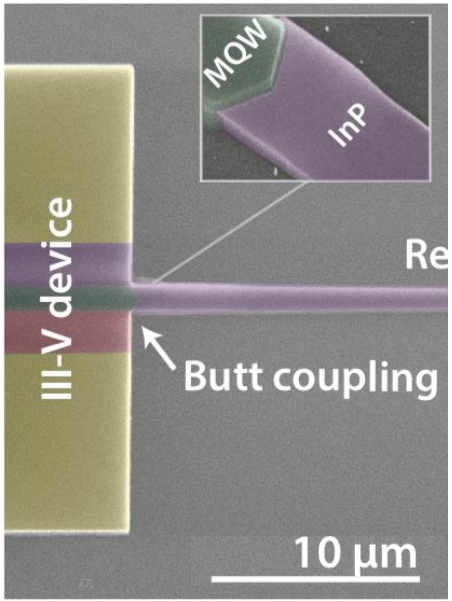
BEOL integratable III-V photodetectors

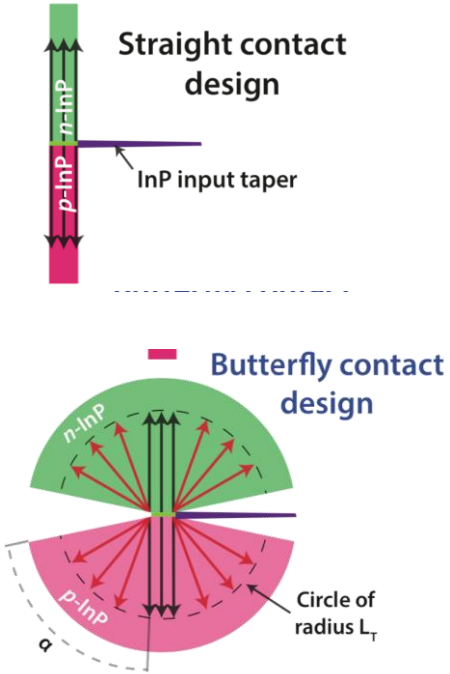
- Very thin ~300nm → enables BEOL CMOS integration
- Based on direct wafer bonding of active layers
- Evanescent coupling to underlying SOI waveguide
- High device responsivity (up to 0.6 A/W)
- Record low dark current (0.1 nA at 3V)
- Ultra low capacitance (0.3 fF/μm at -3V)
- Data transmission at 25 Gbps

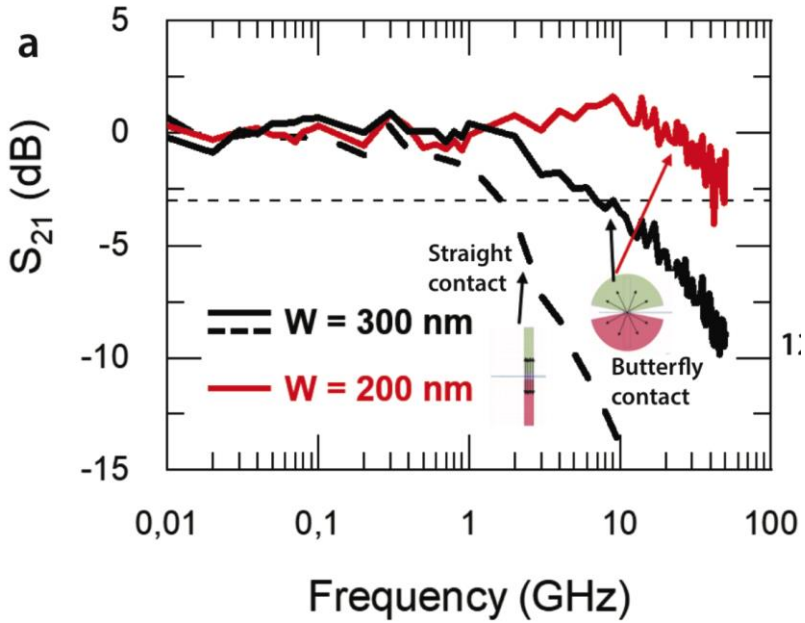


📖 Y Baumgartner et al. IBM, OFC 2019

Improving Device Bandwidth







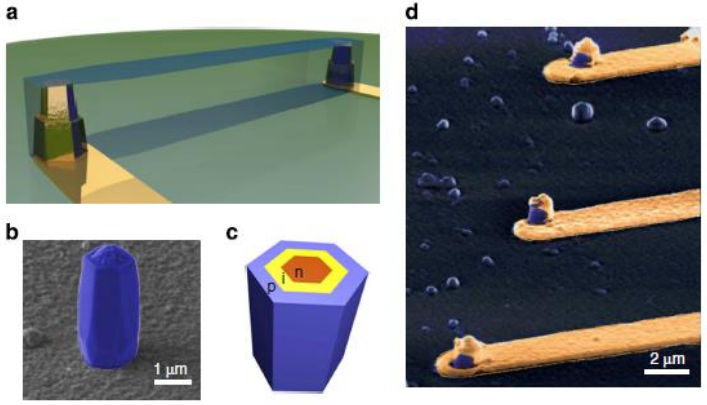
Collaboration with Institute of Electromagnetic Fields (ETH)

- Record bandwidth (65GHz) for III-V photodetectors on Si

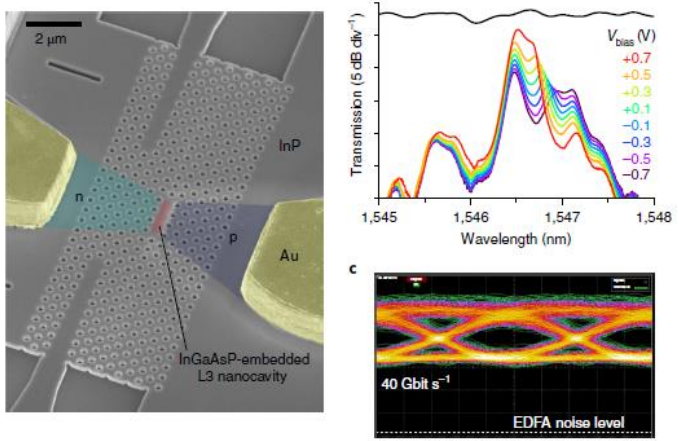
📖 **Y. Baumgartner**, *et al*, OFC, (2019)
📖 **Y. Baumgartner**, *et al,* ISUPT/SSPHF, invited (2019)

Monolithic Scaled III-V PDs on Si

- BEOL and bonded devices for datacom achieve great performance
- But ideally for an on-chip scheme we would like to have dense integration with silicon photonics and devices comparable with transistors
- Local monolithic growth of III-V on silicon would provide that.
- Most devices still immature from a VLSI perspective

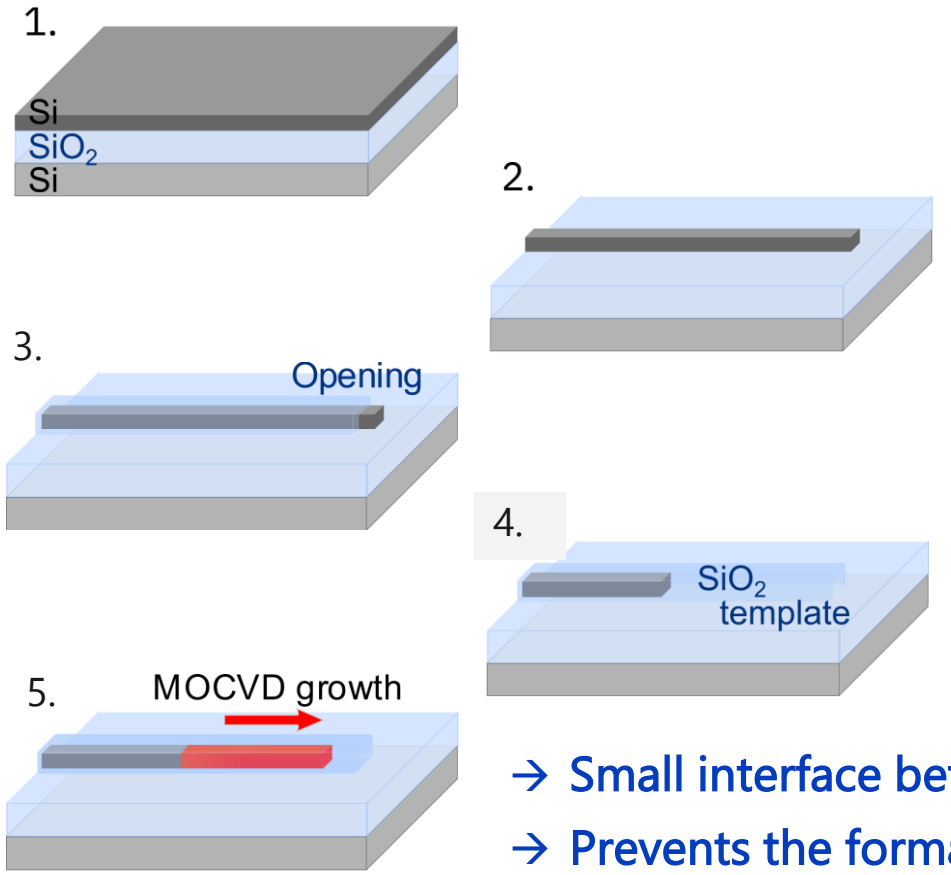


📖 R. Chen et al., Nature Com. 2014



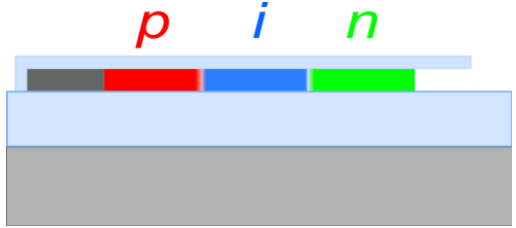
📖 K. Nozaki et al. NTT, Nature Phot. 2019

In-plane Monolithic Integration on Silicon



Template-assisted selective epitaxy (TASE)

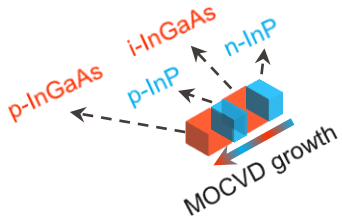
1. SOI wafer
2. Patterning of top Si layer
3. Deposition and partial opening of SiO_2 layer
4. Partial etch of Si
5. MOCVD growth of III-V material



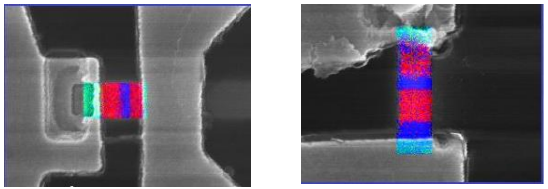
→ Small interface between Si/III-V enables stress relief

→ Prevents the formation of defects

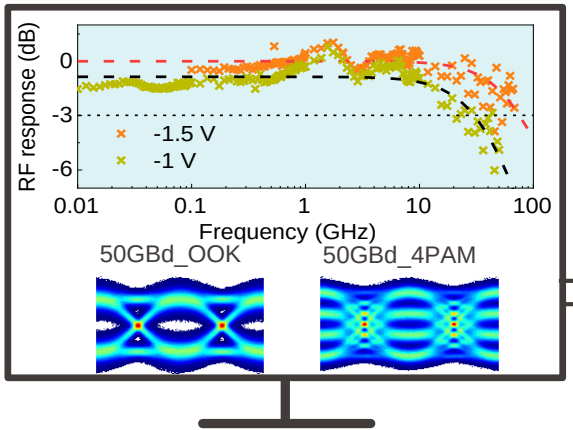
Waveguide coupled p-i-n detector

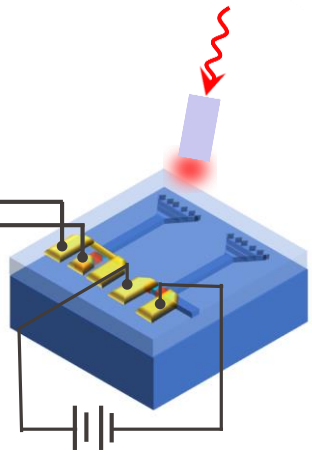


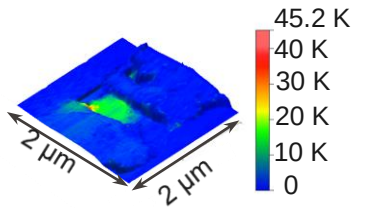
Top-view EDX: Au InGaAs InP



S. Mauthe, ETHZ Thesis Silver Medal







📖 S. Mauthe OFC 2019, 📖 S. Mauthe, Nature Com. 2020, 📖 P. Tiwari, OFC 2021, 📖 P. Wen, Nature Com. 2022

- Si passives and gratings etched in top layer of SOI wafer (220 nm thick Si)
- Seamlessly coupled to SOI waveguides
- III-V active regions self-aligned to Si passives, larger device ~300 x 300 nm^2
- InP/InGaAs/InP heterostructure improves carrier confinement

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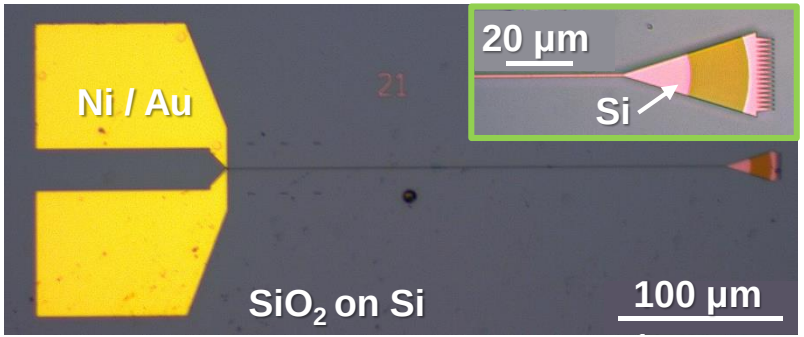
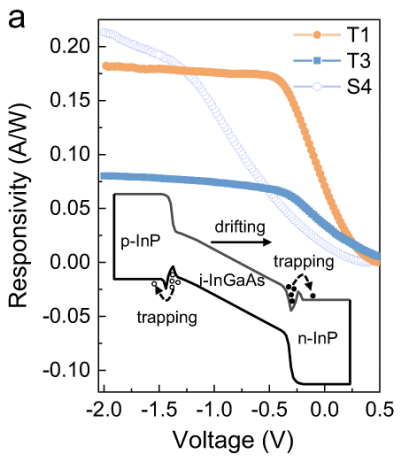
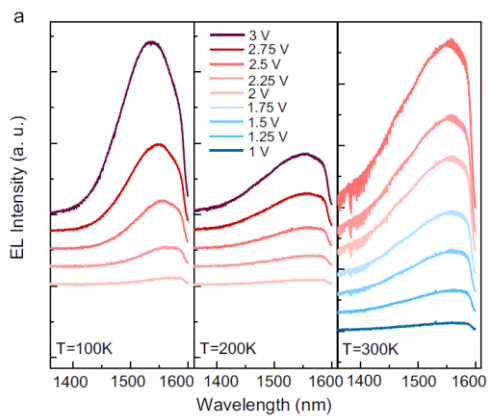
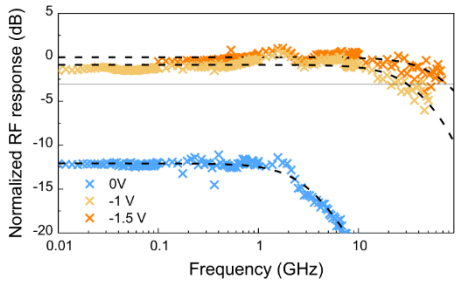
Detector performance

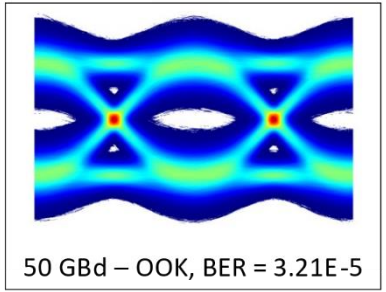






- 3db cutoff frequency reaching 70 GHz
- Data reception at 50 Gbps
- Responsivity up to 0.2 A/W – not accounting for WG→ III-V coupling losses
- LED emission at 1550 nm





P. Tiwari et al., OFC 2021
P. Wen et al., Nature Com. 2022

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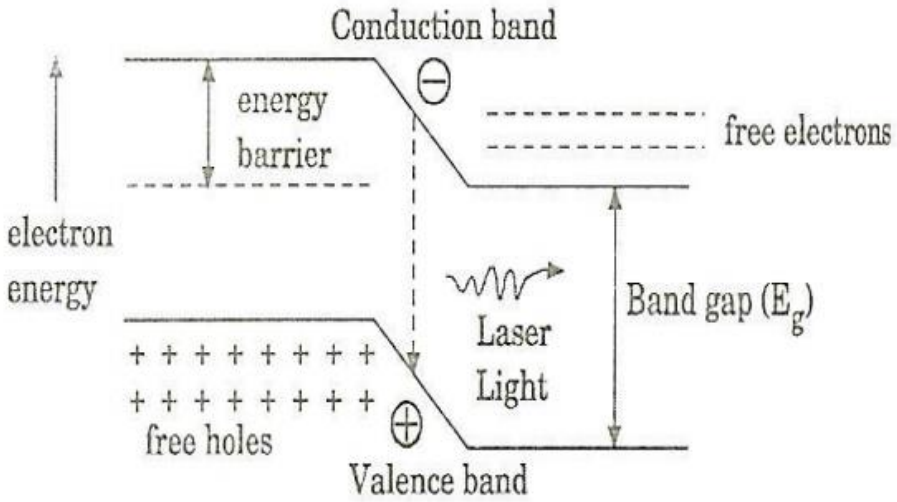
Emitters

Light emission in semiconductors



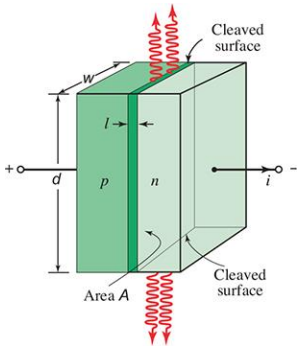
- Carriers are excited in a semiconductor by optical or electrical pumping
- A population inversion is created and an excited electron combines with a hole
- During the recombination process, the light radiation (photons) is released
- The energy of the photon corresponds (roughly) to the bandgap energy

📖 http://www.brainkart.com/article/Semiconductor-Diode-laser--Principle,-Construction,-Working,-Characteristics,--Advantages,-Disadvantages-and-Applications_6886/

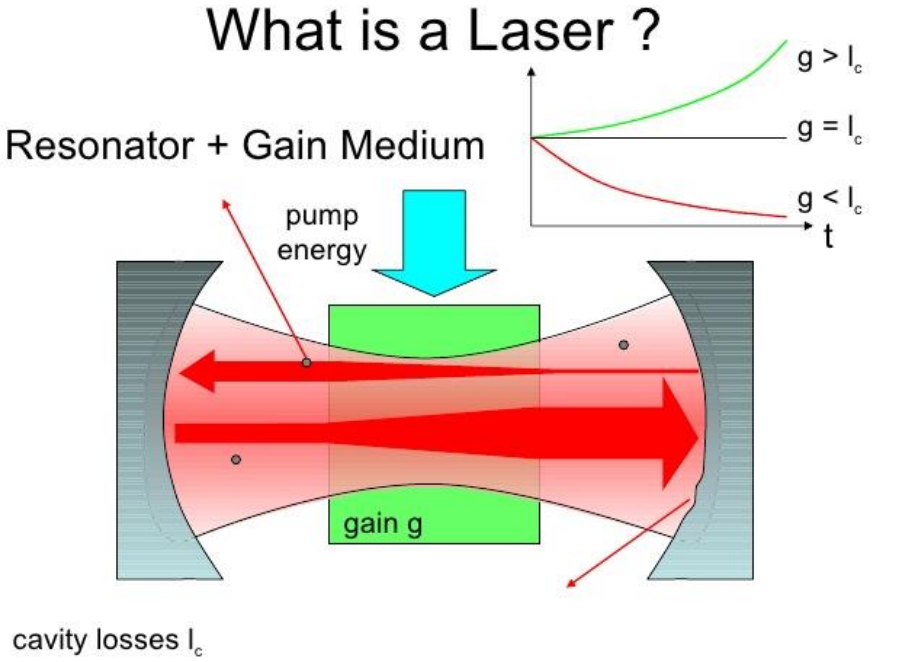
Laser

- Combines a light-emitting (gain) medium and a resonator.
- Threshold: Gain = loss,
- Laser diode is based on stimulated emission, whereas an LED is based on spontaneous emission
- Stimulated emission → emitted photons are identical to the photons already circulating in the cavity

Laser diodes: small, energy efficient, electrically driven, ease of integration with electronics.

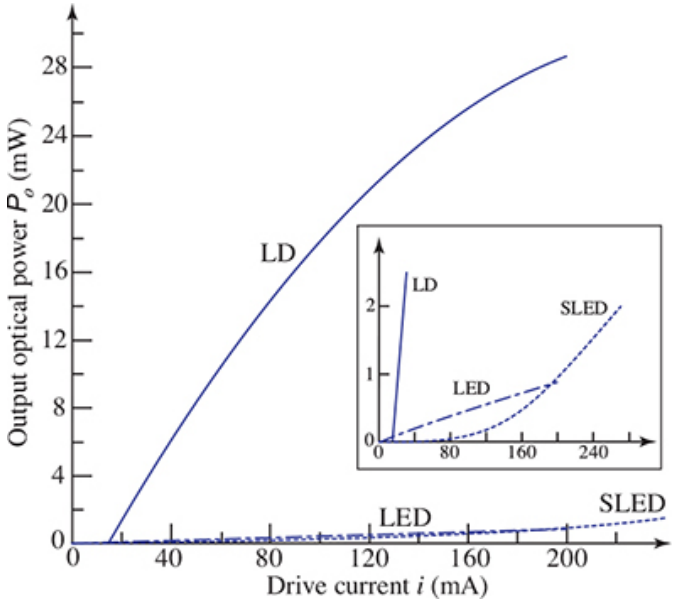


📖 Fundamentals of Photonics, Fig. 18.3-1

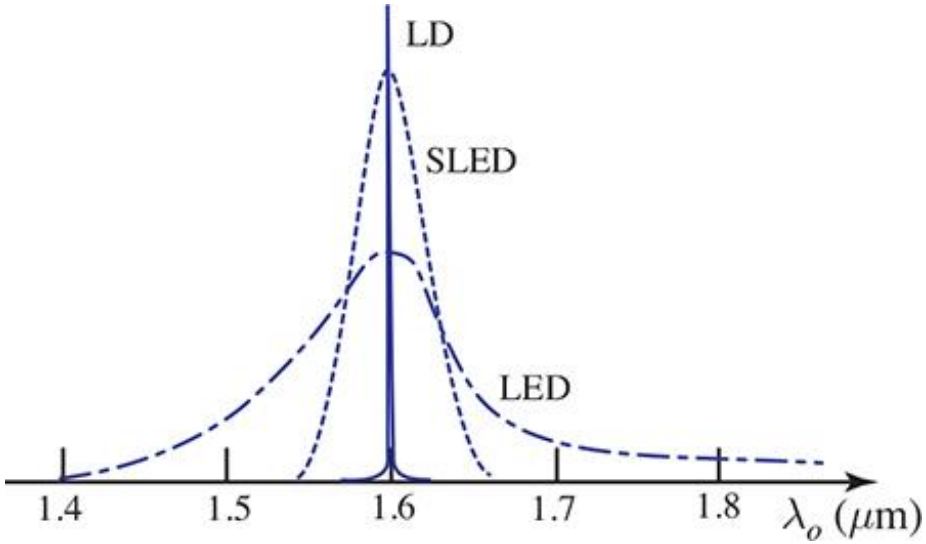


📖 https://www.slideshare.net/dlorenser/part-i-laser-basics-lorenser-2009

Comparison: LED vs Laser



📖 Fundamentals of Photonics, Fig. 18.3-5



📖 Fundamentals of Photonics, Fig. 18.3-7

- All three devices are InGaAsP/InP MQW structures operated at a wavelength of 1600 nm, and at modest values of the drive current

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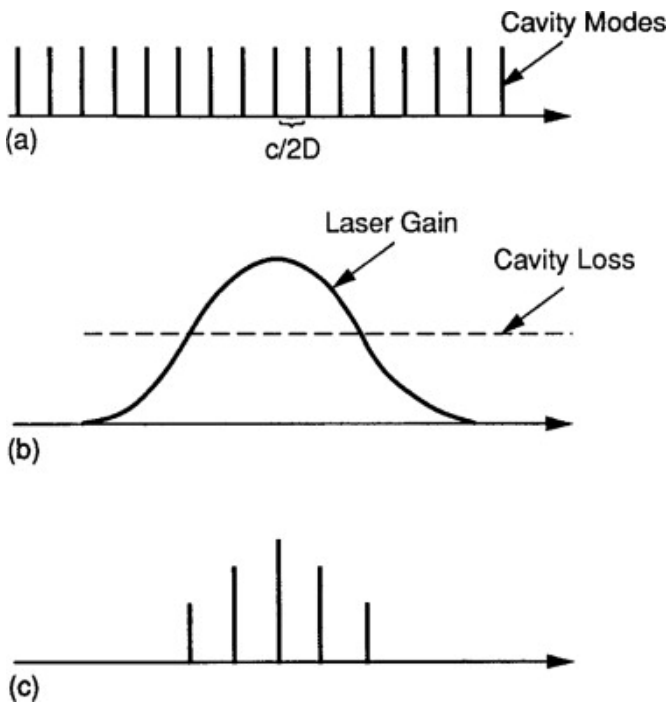
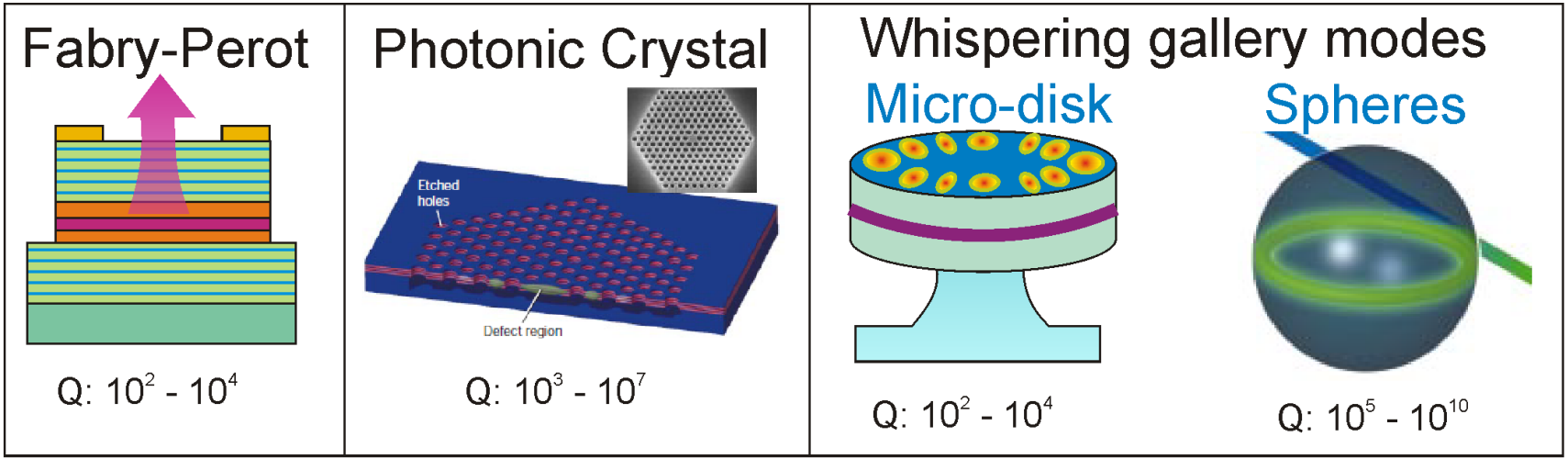
Emission profile



- Cavity modes = feature of resonator.
- Mode spacing: $\Delta\nu = c/(2nL)$
  - L=length, smaller cavities contain fewer modes
- Gain profile
  - Material property, bandgap
  - Number of lasing modes generally increase with pumping

Different types of resonators

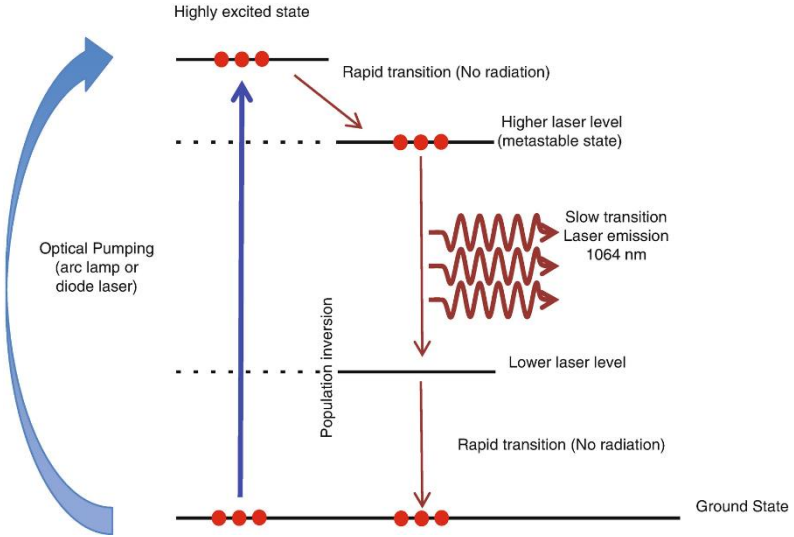


- Quality (Q) factor: the ratio of the peak energy stored in the resonator in a cycle of oscillation to the energy lost per radian of the cycle.
- Higher *Q* indicates a lower rate of energy loss and the oscillations die out more slowly

Pumping method

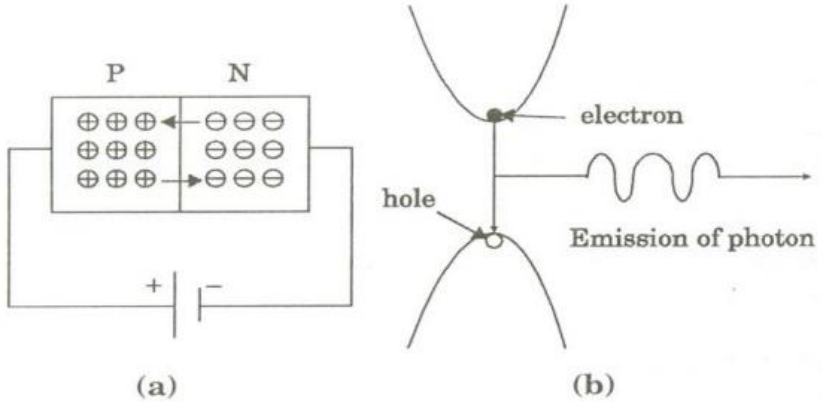
Optical pumping

- $E_{pump\_photon} > E_{emission\_photon}$
- Doesn't require doping profiles or contacts → Usual method for nanolasers



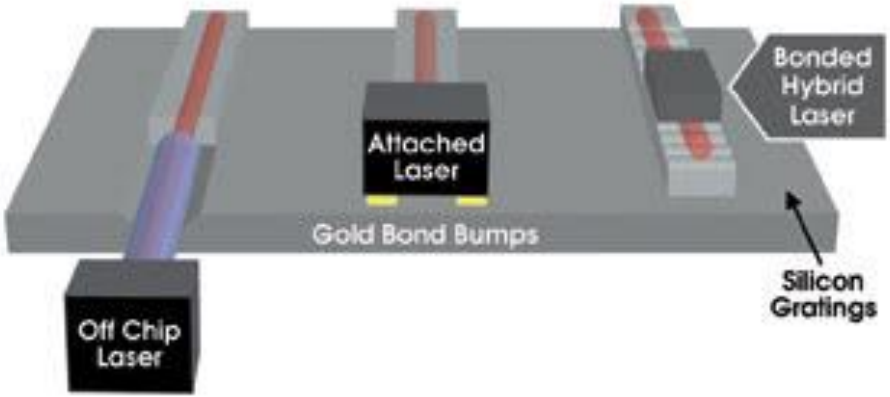
Electrical pumping

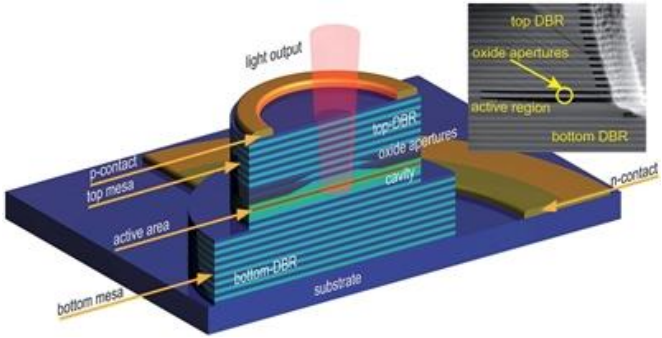
- Forward biased pn-diode
- More adapted to integrated photonics



Standard Laser Integration Approaches

📖 https://www.photonics.com/Articles/A_Hybrid_Silicon_Laser/a27801

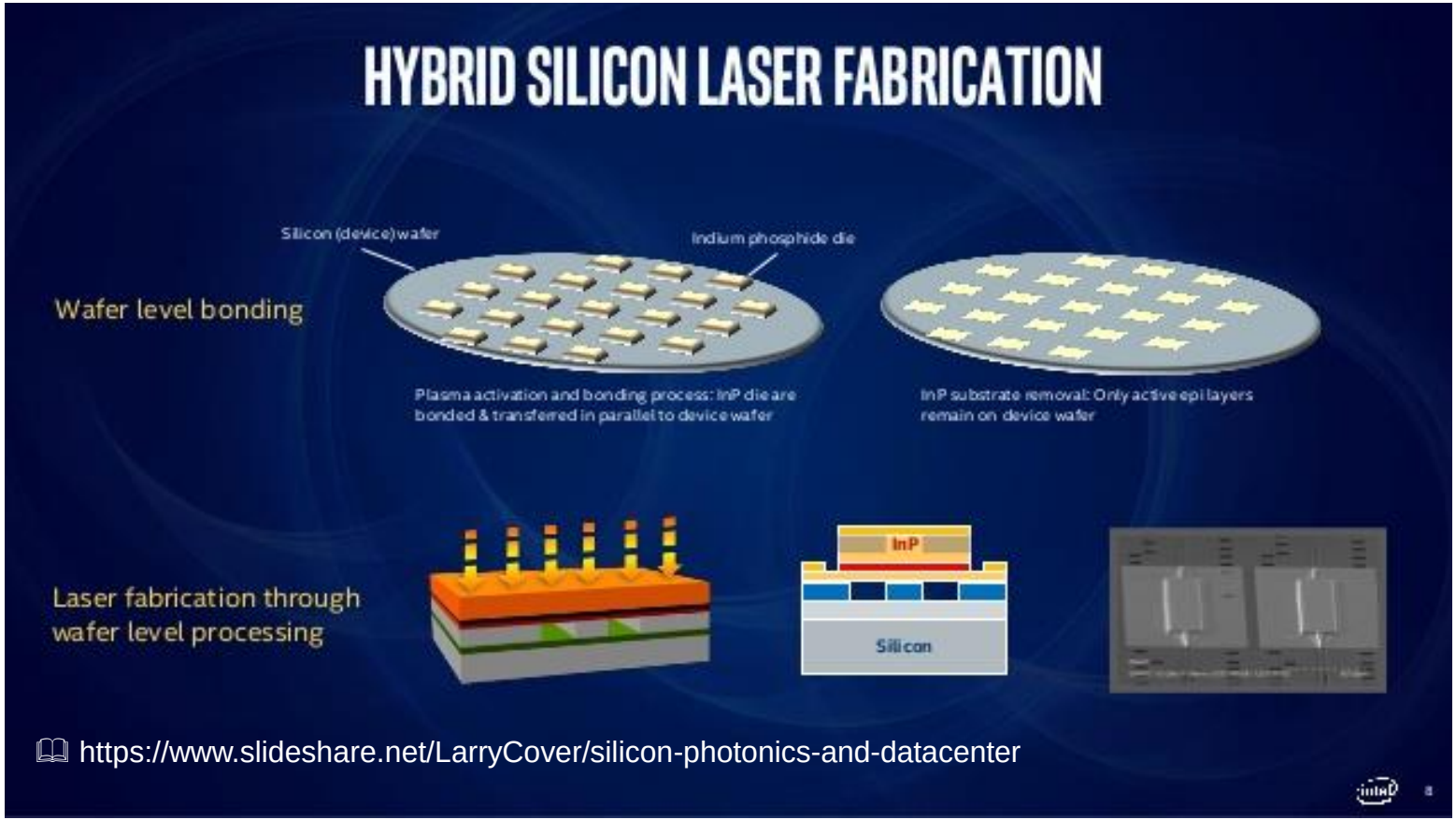




VCSEL – Vertical cavity surface emitting laser

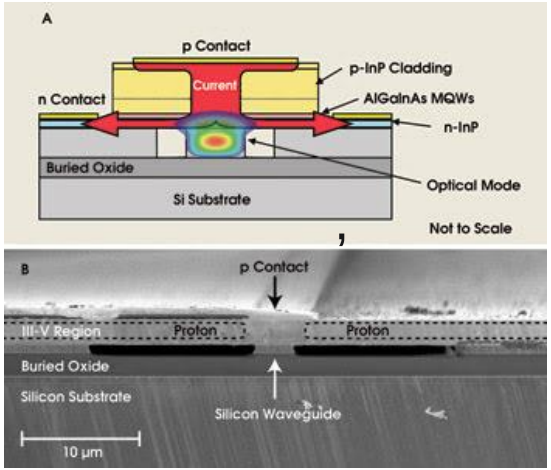
- The laser is the most power-hungry device → good reasons to keep it off-chip
- Single «global laser» signal, possibly with on-chip modulators
- VCSELs – otherwise some of the most scalable lasers, are not suitable for on-chip communication because of the out-of-plane emission → will not be covered here

Intel's approach at hybrid integration



Hybrid Integration

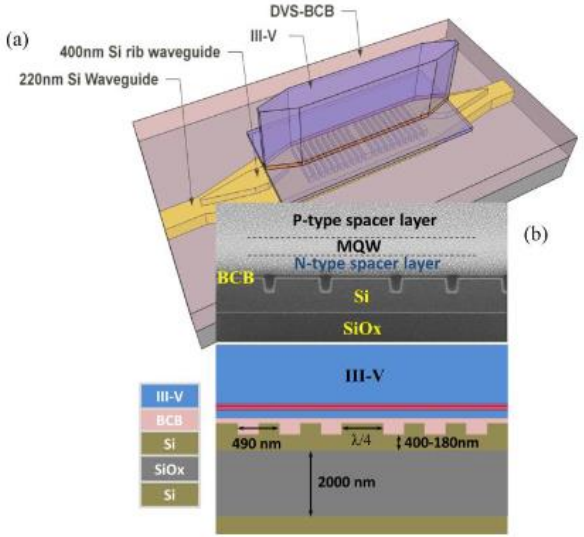
- Bonding of the active III-V MQW stack on top of a SI waveguide



- AlGaInAs layer bonded on SOI
- Length ~800 μm
- Cavity defined by silicon WG → no critical alignment

📖 A.W. Fang et al. *OPT EXPRESS, 2006. Collab. UC Berkeley/Intel*

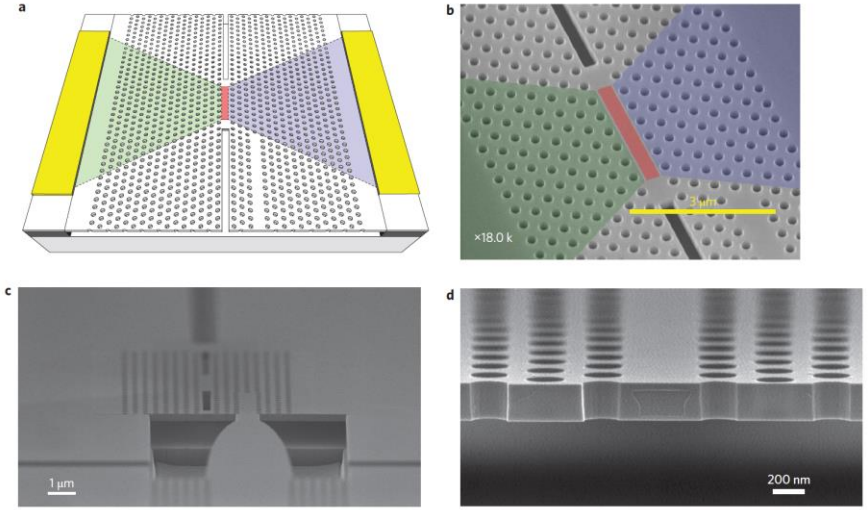
- InGaAs-based MQW stack BCB bonded on Si photonics platform.
- Length of svereal hundred μm's
- Advanced taper structure
- Fiber-coupled output of 14 mW



📖 S. Keyvaninia et al. OFC 2013, *U. Gent/IMEC*

Photonic crystal lasers

- Need low-power and smaller lasers for on-chip integrated communication
- Very high-Q factors achievable
- Lowest power per bit demonstrated
- Usually wafer bonded membranes
- But, although the cavity is small the 2D PhC lattice takes up space
- Often suspended structures → not VLSI compatible

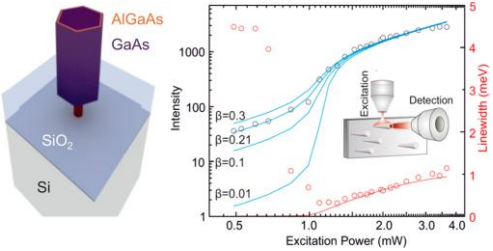


- Length of cavity ~ 3 μm
- Output power of 2.17 μW and an operating energy of ~4.4 fJ/bit

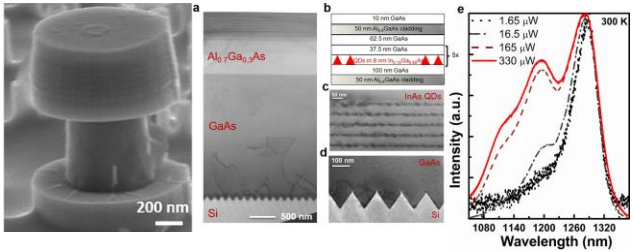
📖 Takeda, NTT, Nature Photonics, 2013.

Monolithic integration of Emitters

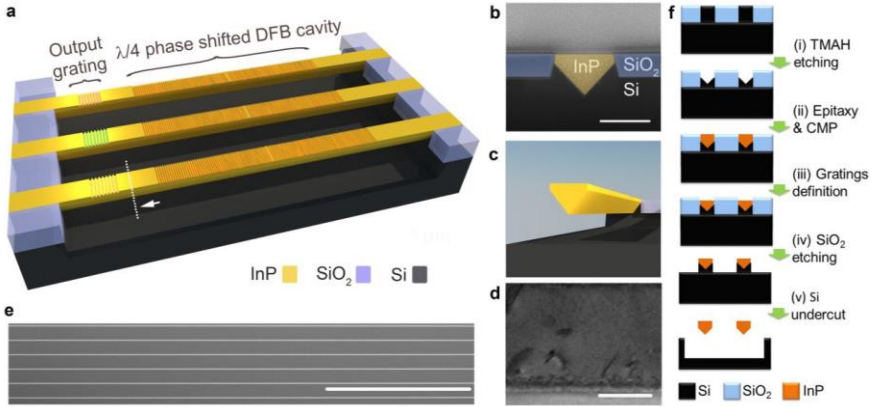
- Growth directly on silicon → most dense integration path.
- But, lattice mismatch makes it hard to achieve high quality material
- Scaled geometries
  - 100s of nms compared to 100s of μm → potential for low power
- Most monolithic nanolasers still only optically pumped
- Unique geometries are hard to contact



📖 Mayer et al. Nano Lett., 2016

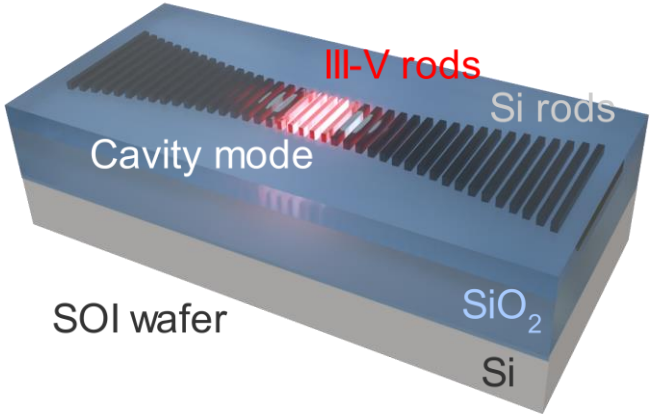


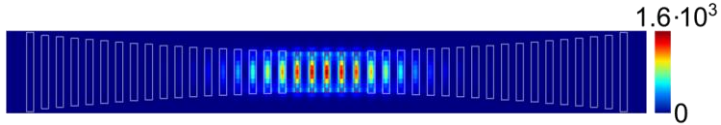
📖 Wan et al. Apl. Phys., 2016

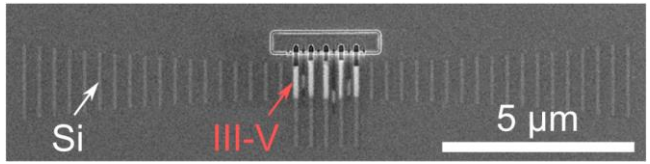


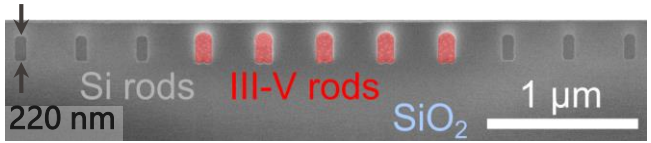
📖 Wang et al. (U. Gent) Nature Photonics, 2015

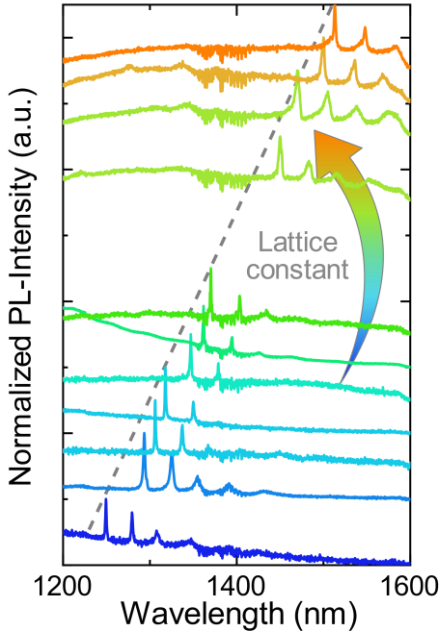
Hybrid Photonic Crystal Cavities











→ **Independent gain and resonant structure optimization**

→ **Emission in the desired telecommunication band**

📖 S. Mauthe et al, IBM, Nano Lett. 2020

Partial Summary: Devices

- A direct bandgap is required for emission, whereas detectors are possible with an indirect, but less efficient
- Ge is the SoA solution for detectors.
- Wafer bonding on hybrid architectures is the most comment technique for co-integration with Si WGs – most of these devices are on the scale of 100s of μms
- Scaled lasers are need to reduce power consumption, but most approaches are immature
- Monolithic approaches are required to
  - Provide denser integration with silicon passives and electronics
  - Down scaling of dimensions to reduce power consumption and enable large scale integration (number of devices)

Summary

What I was working on recently

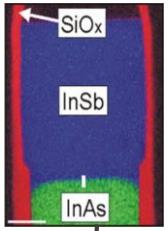
Heinz Schmid

Epi- Growth

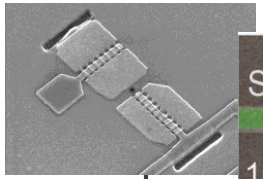
Applications

Time 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022

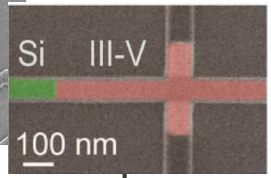
InSb/ InAs first trials



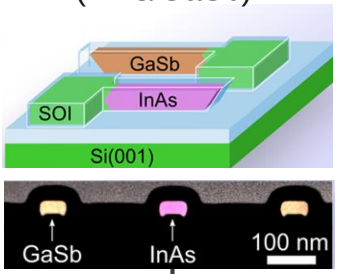
CELO growth



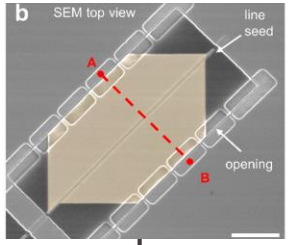
Arbitrary shapes



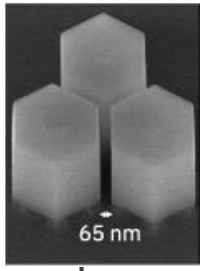
Co-integration (InAs/GaSb)

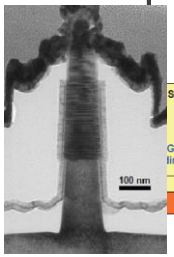


Crystal phase control (on InP)

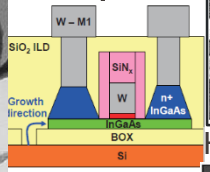


Zipper-ELO (on InP)

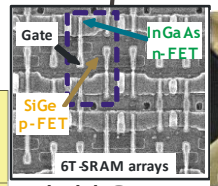




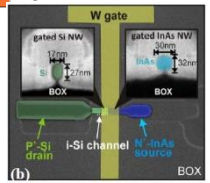
P-TFET InAs-Si



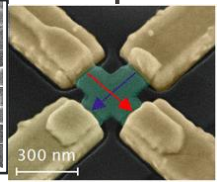
MOSFET InGaAs & InAs



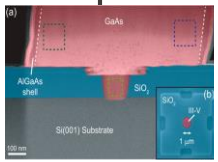
Hybrid SRAM



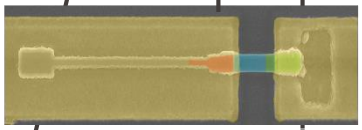
C-TFET



Ballistic NW transport

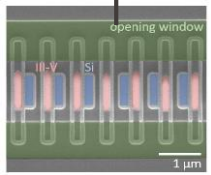


Microdisk lasers

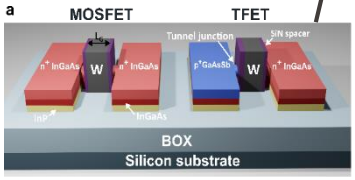


Monolithic detectors

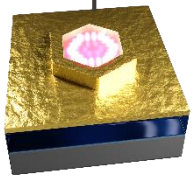
Hybrid PhC



Topological laser



Hybrid TFET/MOSFET platform



Cavity scaling

Thank you for your attention – Questions?

PSI team 2022

IBM team 2020

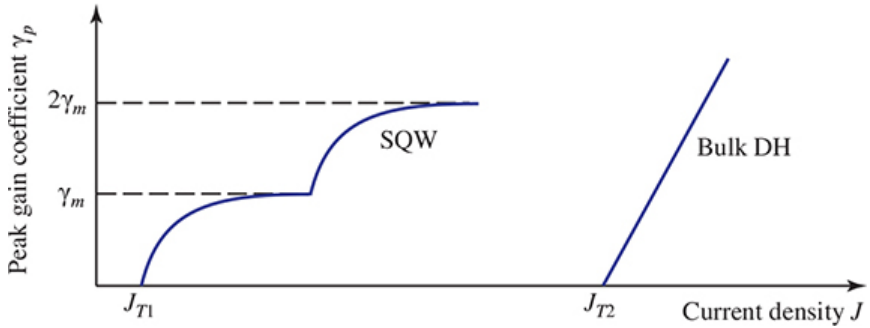
Funding
EU FP7: E2SWITCH
EU H2020:CONNECT, DIMENSION, INSIGHT, DESIGN-EID

Back-up slides

Quantum well vs. Bulk Double Heterostructure lasers

Advantages of QW lasers

- Smaller threshold current density
- Larger external differential quantum efficiency
- Larger power-conversion efficiency
- Narrower gain-coefficient width
- Smaller laser-mode linewidth
- Reduced temperature dependence
- Faster response and thus greater modulation frequencies



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